A NEW APPROACH FOR TOPOLOGY SELECTION OF ANALOG CIRCUITS

A thesis submitted
in partial fulfillment of the requirements
For the degree of

MASTER OF TECHNOLOGY

By

ARUN KUMAR SHARMA

to the

DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY, KANPUR
FEBRUARY 2000

CERTIFICATE

This is to certify that the work contained in the thesis entitled "**A NEW APPROACH FOR TOPOLOGY SELECTION OF ANALOG CIRCUITS**" by **Arun Kumar Sharma** has been carried out under my supervision and that this work has not been submitted elsewhere for the award of a degree.

Dr. BAQUER MAZHARI

Assistant Professor,

Department of Electrical Engineering,

Indian Institute of Technology, Kanpur.

February 2000.

Dedicated

To

My Parents

ACKNOWLEDGEMENT

I take this opportunity to express my sincere gratitude towards Dr B. Mazhari without whose guidance this thesis work would have not been in the present form. I appreciate his invaluable motivation, encouragement and guidance in making this thesis a success.

I would like to thank Dr. K. Deb, department of ME, for providing me the needed help for my work. I would further like to thank Dr. A. Dutta, department of EE whose courses helped me in improving my knowledge.

Last but not the least I would like to thank almighty God and my family members who made me reach this stage where I could undertake the work of this magnitude.

Arun K. Sharma
(ARUN KUMAR SHARMA)

ABSTRACT

Owing to steady increase in the number of new application specific integrated circuit (ASIC) designs that include analog functions and their increasing complexity, the need for analog computer-aided design (CAD) tools is being urgently felt. The bulk of the research in the area of the *analog design automation* is devoted to the issues of "*parameter selection*", i.e., selecting optimum device sizes and bias points to meet the specific targets. Although "*topology selection*" is crucial in designing the high performance analog circuits however little work is reported in this area. In the present work, a new approach is presented for selection of topology from a fixed set of alternatives. The basis of the new approach is in the new definition of a topology, which is characterized as a set of analytical equations that describe the constraints among the specifications. Topology selection is done by determining the topology, which while satisfying all the constraints, has minimum area or some other metric. It is shown that this approach encompasses within it the traditional qualitative rule-based topology definition and selection methods. The validity of approach is demonstrated with the help of various op-amps like, Miller compensated complementary metal oxide semiconductor (CMOS) operational transconductance amplifier (CMOS OTA), simple CMOS OTA and Folded cascode CMOS OTA.

CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1

INTRODUCTION

1.1 Background

Nature is mostly analog. Interaction with nature is therefore inevitably analog. The advent and evolution of computers and digital signal processing methods resulted in a tremendous potential for processing power which, in contrast to nature, could only process digital signals. Analog interface circuits have, therefore, become vital and indispensable parts for most of the digital circuits. They provide the necessary signal conditioning and modification such that they can be processed digitally. Interface circuits vary widely depending on specific functions and applications, such as data acquisition systems, A/D and D/A converters, particle and radiation detection circuits, automotive electronics, biomedical instrumentation and control circuitry, robot sensing, preamplifiers, power drivers, etc. [1]. During the last few years, a revival of industrial interest in analog integrated circuits has resulted in a new series of circuit functions and higher levels of performance accuracy in the areas of microprocessor supervisory circuits, power supply ICs, battery back-up switches, massively parallel analog signal processors (neural networks), and switched capacitor filters. Analog circuits are the main signal processors in applications where area,

power, and high frequency operation are the performances of concern, vastly outperforming their digital equivalents.

Economic and other factors favor the co-existence of analog circuits either interfacing or main signal processing circuits and digital circuits on to the same die. Application specific integrated circuits (ASICs) that are designed according to customer specifications move therefore steadily towards the integration of complete systems on a single chip (SOC). It has been reported that in 1990 approximately 60% of all CMOS and BICMOS ASICs were mixed analog and digital [1].

The growing requirements for single-chip mixed VLSI systems, together with the trend towards smaller feature sizes and higher scales of integration, have brought about new dimensions in the circuit design complexity. Digital designs have been largely automated with sophisticated CAD tools exploiting hierarchy and structured abstractions. In contrast, analog design is commonly perceived to be one of the most knowledge-intensive tasks and analog circuits are still designed largely by hand by experts, familiar with the tradeoffs involved in the performances and integrated circuit fabrication processes. Analog Design is a human process that suffers from an identity crisis largely because of convention of categorizing circuit design as either digital or analog. In fact recent preponderance of digital circuit design in the electronics community has resulted in a Boolean definition for analog circuit design.

$$ANALOG = \overline{DIGITAL}$$

Or anything, which isn't digital design, must be analog design [38]. This simple expression highlights the difficulty of the analog design automation in terms of scope. The techniques needed to build good analog circuits seem to exist solely as expertise invested in individual designers.

The problem of analog synthesis may be defined as one of selecting circuit topology, sizing the composite components, and laying out the structure in a manner that realizes the required functionality an meets the desired performance criteria. While objective is easily stated, the design of analog integrated structures that meets such criteria are not. To appreciate the complexity of analog designs and automation thereof, it is constructive to compare analog and digital design mediums. The following observations may be made [6]:

1. In the digital domain, there are typically only three main performance measures of interest, namely area, power and delay. In contrast, performance attributes typical of analog circuits are numerous and depend on functional block of interest.
2. The digital signal may be simply characterized as having two unique logic states. A consequence of the discrete binary levels is that digital signal is subject to formal mathematical treatment using modulo 2 arithmetic and state variables. The analog signal, however, can carry information in a variety of forms. The amplitude of incoming signal carries vital information in case of analog –to-digital converter. Alternatively phase lock loop systems process phase information and are indifferent to signal amplitudes.
3. In the digital domain, system performance may be readily expressed as a linear function of sub-system performance with the little loss in modeling accuracy. In the analog domain, system performance is typically a nonlinear function of lower level attributes.
4. With the inclusion of simple back annotation schemes, digital design methods such as standard cell and gate array permit layout to be considered independent of circuit topology selection and component sizing. In the analog domain, net parasitics can play a dominant role in determining attributes of high performance analog blocks. The use of standard cell libraries is not practical due to many divergent performance measures typical of analog systems. Critical layout parasitics must, therfore, be considered commensurate with topology selection and component sizing.

Typical staring point of an analog design, are a circuit topology and a set of parameters obtained from the designer's experience. Then several simulations and redesigns are carried out until an acceptable solution is achieved. This redesign process is very time-consuming task In addition designer's experience is required to interpret the results obtained from the simulation and to modify the design parameters in the proper direction [2]. The increasing demand of application-specific IC's (ASIC's) that are entirely or partly analogic, makes necessary the development of CAD tools, which can aid in decreasing the design time, allowing nonexperts to design complex analog circuits.

CAD tools specifically tailored to analog integrated circuit design promise to improve the design process in a variety of ways [5], which are detailed below.

1.) By shortening the design times.

2.) By simplifying the design process: As a consequence, more designers, starting from novices to experts, will be able to design standard analog circuits.

3.) By improving the likelihood of error-free designs: Automating error-prone design tasks reduces the probability of making errors, and, therefore, decreases the design cycle/success ratio.

4.) By retaining expert design knowledge: The knowledge acquired by the design systems can be used for subsequent designs. It can be conveyed to novice users in the form of design examples, explanations of behavior, suggestions for modifications, and/or conclusions.

The designer first selects a circuit topology among a set of fixed alternatives topologies, in order to achieve higher performance for a particular application. The second step, after the topology of the circuit and component types are fixed, consists of assigning values to the circuit parameters (e.g., widths and lengths of MOS transistors, resistor and capacitor values, bias voltages and currents etc.) while satisfying the desired performances. The optimized circuit then needs to be transformed into a layout [25].

Existing CAD tools mainly focused on the parametric optimization phase. Early optimization tools used a step-by-step procedure previously determined by an expert designer [8]. Final design may be considered as a starting point for manual parameter adjustment. An early review of these techniques can be found in [9]. Experts rely on years of experience to guide the selection of circuit topologies and parameters for those topologies [3]. Considerable work in the area of has been devoted to the issues of *"parameter selection"*, i.e., selecting optimum device sizes and bias points to meet specific performance targets. However, *"topology selection"* is crucial in designing the high performance analog circuits; some performance specifications are vastly easier to meet if we allowed to change not only device sizes, but also the number, type, and interconnections of the devices.

1.2 ANALOG DESIGN APPROACHES

An overview of various approaches used for "parameter selection" part of analog design is given as follow. Figure 1.1 depicts schematically a classification of the various analog circuit design approaches.

1.2.1 Layout-Based Design Approach

This approach is an adaptation of extensively used standard cell, gate array and parameterized cell methods found in digital domain. In this approach designs are controlled to a large extent by layout, so referred to as *semi-custom bottom-up approach* [1].

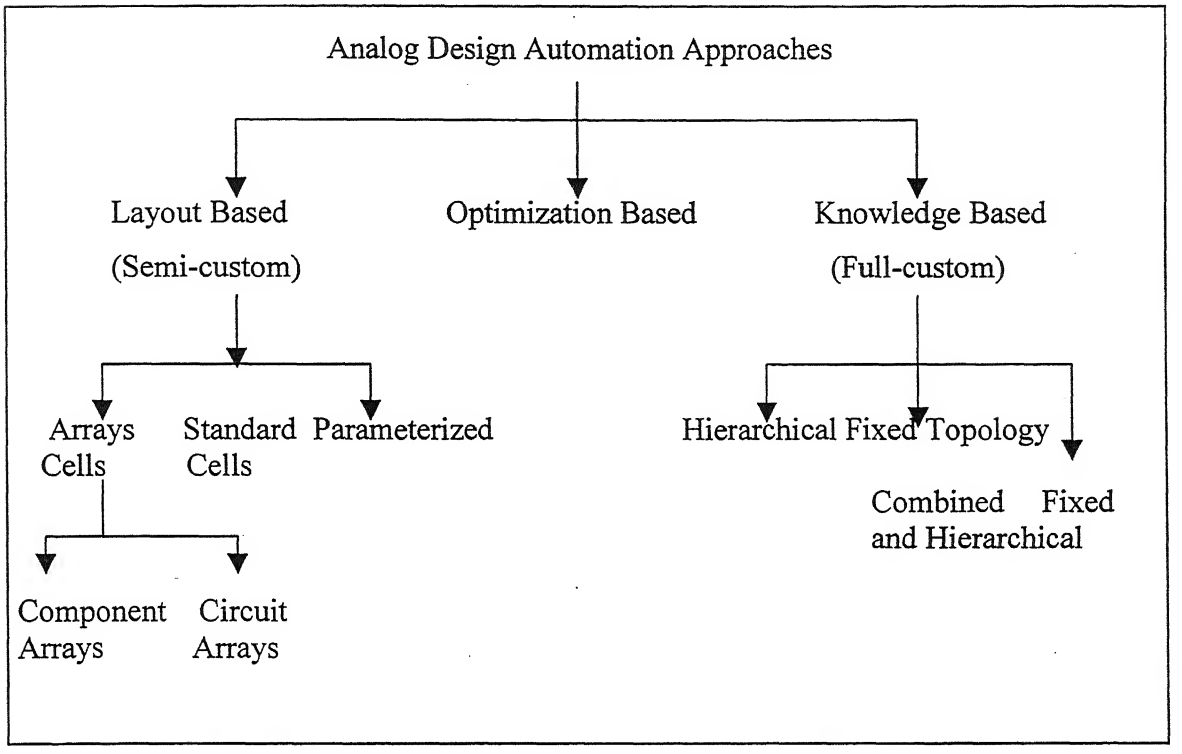


Fig 1.1: A classification of the various analog IC design automation approaches (taken from [1]).

Analog arrays are pre-designed and laid-out blocks of different sizes, configurations and levels of complexity, varying from single component arrays to circuit arrays. The required functions are designed by appropriately programming one or more levels of interconnect. This approach does not provide the necessary design flexibility required for high performance analog circuits. Not only there is a limited range of active and passive components available, but also their values are of a

limited range. Thus, analog arrays can realize only a small number of discrete points within a wide and continuous performance space. Arrays are not very much cost-effective in terms of silicon usage, since any unused components or circuits in the array simply waste silicon area without providing any function at all. Standard cells address the problem of silicon usage in a better fashion than the arrays. They are pre-designed and laid-out blocks of varying complexity that resides in the database of the DA system. The required function is implemented by assembling the necessary cells and then by placement and routing. Although the use of standard cells may have been successful in the digital domain, it has quite restrictive use for analog circuits, since it is extremely difficult to configure and maintain a rich enough library of cells in order to accommodate a wide spectrum of possible applications. Both arrays and standard cell libraries are very brittle since they track the fabrication process very poorly. A number of CAD systems that use standard cell techniques are reported in the literature [6-8].

The use of analog parameterized cells is an alternative layout-based design approach. parameterized cells are similar to the standard cells, but with some additional flexibility gained by allowing some customization of the cells (or part of them) according to the required function. The degree of flexibility provided is directly dependent on the sophistication of the respective module generator - the piece of code that generates the layout of the cell given a set of input parameters. With application of this approach, AIDE2 has demonstrated the design of several circuits e.g., amplifiers, integrators, switched capacitor filters, and A/D converters [1].

1.2.2 Knowledge-Based Design Approach

Knowledge based systems exploit domain knowledge to design analog integrated circuits, and they address the design task in a full custom way, thereby allowing for maximum flexibility and a potentially better coverage of the circuits' performance space. So far, the main design philosophies that have evolved and prevailed are the *hierarchical* and the *fixed-topology* approaches.

Hierarchical Approach

The hierarchical design approach has been successfully applied to digital design automation, and is now seen in analog design also. The idea involves breaking of the required circuit (or system) into smaller distinct parts. Each of these parts is assigned a set of specifications which, if met, then the combination of these parts will

yield the desired circuit performances. To be able to carry out such partitioning of circuits and decomposition of specifications, good domain knowledge is required, and generally, it is in the form of design equations and heuristics. These systems maintain the greatest degree of freedom and thus a small architecture library can lead to a large number of different topologies with wide performance spectra. The various systems use this kind of approach are OASYS [9], BLADES [10], An_Com [11], etc.

Fixed Topology Approach

This method employs a sizing method in order to compute appropriate sizes for the devices within a given fixed circuit topology. These fixed, unsized, device level circuit topologies are stored in a knowledge base together with the necessary domain knowledge for dimensioning the devices. The nature of the domain knowledge depends on the method of computing device sizes. Some of the systems reported in literature that follow this approach are IDAC [12], OPASYN [13], OAC [14].

Combined Hierarchical and Fixed Topology Approach

There is some knowledge-based design methods, which combine features of both the hierarchical and fixed topology approaches. ASAIC [15] is a system that fits into this class of design systems, since it puts together the circuit topology in a hierarchical manner whereas the design of device dimensions of the topology is performed in a manner that resembles fixed topology systems. CAMP [16,17] is also one of such systems that designs a circuit first by viewing it as having a fixed topology, and, then, by allowing modification to the various sections of the initial topology in order to meet the required performance specifications. ISAID [1,18] uses the concept of combined hierarchical and fixed topology approach but it encompasses a circuit generator and a circuit corrector. Circuit generator is based on newly developed methods that are used to handle hierarchical generation of topologies. The circuit corrector is an application of qualitative reasoning, which, analyses performance trade-offs without iterative simulation, thereby modifying topologies suitably. However, these are not as flexible as the hierarchical systems.

1.2.3 Optimization-Based Design Approach

The optimization-based design approach uses recent advances in the optimization theory and algorithms, and relates these to the parametric optimization of analog integrated circuits. A survey of the various techniques used for optimization of integrated circuits can be found in the literature [19, 20]. The synthesis problem is formulated as a mathematical programming problem. Circuit performances are considered as objective functions, which are to be minimized or maximized subject to a set of specification constraints.

The very first attempt towards analog design automation were numerical optimization based. Systems such as DELIGHT.SPICE [21], ECSTACY [22], and the more recent ADOPT [23], consider the sizing of transistors of a given circuit topology as an optimization problem. Typically, these systems employ optimization algorithms to iteratively adjust transistor sizes in order to meet user-input constraints and objectives.

Systems based on numerical optimization techniques are independent of the actual circuit used, the technology, and the fabrication process. In optimization techniques circuit designer has to specify a good starting point for the optimization algorithm. A bad starting point may lead to some local minimum, potentially rendering a good circuit useless. Simulated annealing and random multi-start techniques attempt to overcome this problem, but they are often computationally more expensive. The user has to have a certain amount of circuit design expertise in order to efficiently use such a system. Such design expertise is particularly important if the designer has to define the designable parameters that the optimizer has to vary in order to optimize circuit performances.

To avoid the time consuming and expensive simulator inside the optimization loop, several attempts have been made. Instead, simplified but sufficiently accurate analytical models that predict circuit performances are used inside the optimization loop. These approaches are referred to analytical equation based optimization approaches. A number of prototypes came out in recent times using this type of optimization techniques are OPASYN [13], STAIC [5], FPAD [25], [27], FASY [2].

In all optimization techniques, it is very crucial to formulate the problem in a right manner, and use an optimization algorithm that reflects the user's intentions as accurately as possible. These are also not easy and obvious tasks. Most

of the optimization methods available are very rigid and often difficult to adapt to the design problems without loss of accuracy. Consequently, most optimization techniques have the limitation of using rigid optimization problem that is too restrictive, thus eliminating or reducing the possibilities to arrange for trade-offs, which are an important factor in the overall design process.

1.3 Topology Selection Approaches

To date proposed analog synthesis strategies have relied on a limited set of approaches to perform the topology selection. These approaches force the user to make the topology selection, employ heuristics to guide topology selection, search exhaustively through all available topologies, or alternate iteratively between topology selection steps and parameter selection steps for various portions of the circuit. Experts may select an existing topology based on prior experience, fits new application. Or they may modify one that almost fits by enhancing specific performance characteristics by trial and error, which often require many design cycles. Creating an entirely new topology is quite difficult. Experience about topology selection is a type of knowledge, which is difficult to capture, as it is qualitative and even changes from one designer to another.

In analog cells, same function can be implemented using different connections of different number of components [3]. Analog circuits have a hierarchical nature to them in that they can be decomposed in sub-cells, which can be further decomposed into components like transistors. Each sub-cell can be implemented in various ways. The total number of topologies therefore, can be combinatorially large because topology choice for one subcircuit can be combined with topology choices for other subcircuits. Which topology is optimal or even feasible will depend upon the sizes of the device chosen for that topology, and this in turn depends upon the specifications. It is hard therefore to make conclusions about a particular topology without having determined the sizes of the devices of that topology. In worst case, it might be necessary to size all the topologies to determine the one suitable for a particular set of specifications.

A new generation of circuit synthesis tools have emerged that, instead of using circuit simulation, employ analytical equations as behavioral modals to predict the

performance of analog circuits [31]. IDAC [12], the first commercially available synthesis tool for general analog cells like op amps and comparators, require human designer to choose one from a set of available topologies and then follows a procedural routine created by an expert analog designer to perform coarse parameter selection. Fine parameter selection uses numerical optimization based on topology-specific circuit simulation. IDAC does not address the problem of automating topology selection. A hallmark of expert analog designer is the ability to choose from a wide variety of topologies in response to different performance requirements. Therefore, it is very important to consider design automation methods that can address the topology selection problem.

OASYS [9], developed at Carnegie Mellon University, approaches the goal of simultaneous topology selection and device sizing. It walks down a hierarchical decomposition of an analog cell, alternatively selecting topologies and translating performance specifications from each level to next lower level, and backtracking to handle design failures. This results in a depth-first search through the space of possible topologies. Although OASYS can automatically design a wide variety of topologies, creating the topology, specific design knowledge – especially the knowledge required for backtracking – is very difficult and time consuming. By recasting circuit design as a sequence of alternating topology selection and translation steps, it loses the easy ability to implement design tricks that jump across many levels of hierarchy. Thus with OASYS we lose a "flattened" view of the design in which all details of individual devices are simultaneously exposed, and independently changeable. Experts use such tricks to push the circuits close to limits of achievable performance (simultaneously exploiting tricks involving topologies, sizing, layout, and process). Since hierarchy explicitly prevents the design plan for one module from depending upon details of how other modules are implemented, so this approach may not be able to reach such extremal points in the design space of a given block.

OPASYN [13], uses heuristic rules to choose a topology from a set of available device-level schematics and then uses numerical optimization to perform parameter selection using equations that predict the circuit and subcircuit performance. Strategy used has been devised based on the aforementioned observations. A decision tree has been defined based on some key design specifications such as general application area, open-loop gain, power supply rejection ratio (PSRR), or fully differential topology requirement. The leaf nodes in

this tree correspond to proven op amp topologies commonly used in many applications, and corresponding design knowledge is stored in the database. Searching for a suitable topology starts at the root of decision tree; nodes of the decision tree are checked in turn whether some subtrees can be pruned away (eliminated from further consideration) based on the range of given specifications. The unpruned leaf nodes are forwarded to the optimization module. HECTOR [47], ISAAC [30] uses a "hierarchical, interactive and expert-system assisted" approach to construct circuit

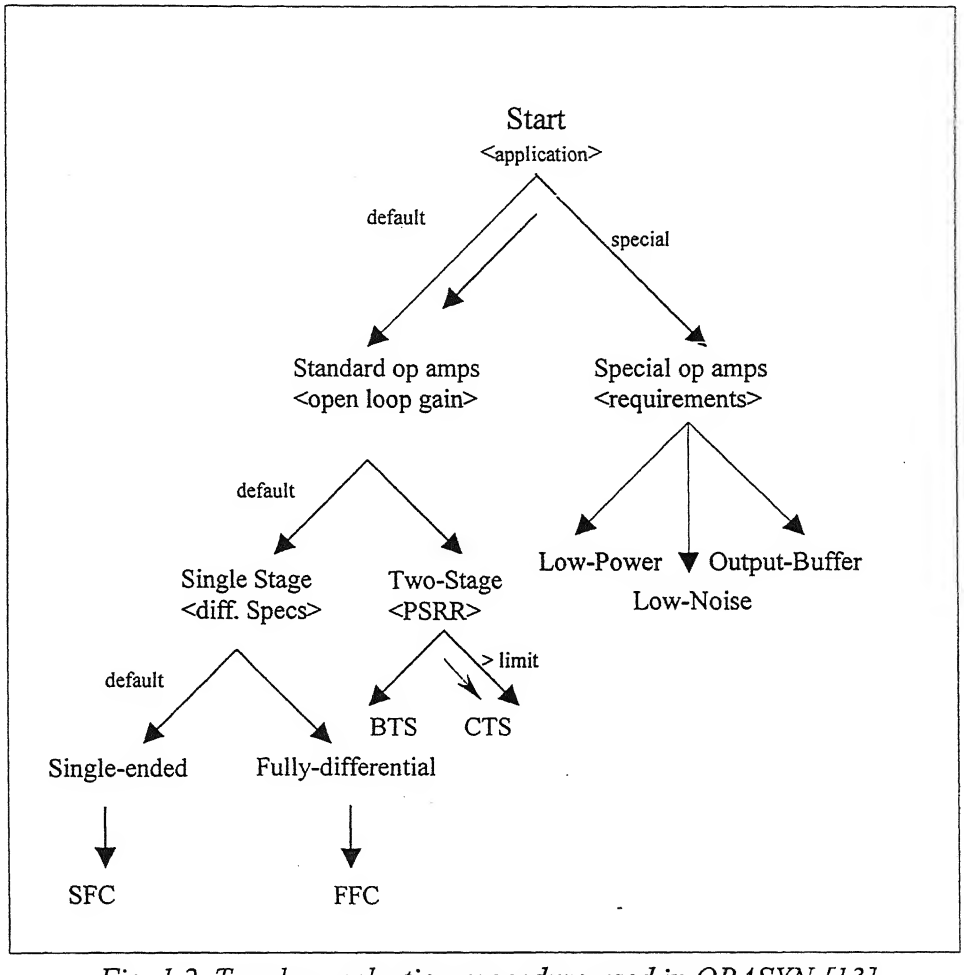


Fig. 1.2 Topology selection procedure used in OPASYN [13].

topologies from a library of basic building blocks. In both these approach's, topology selection employs heuristics which must be provided by expert analog designer. However, it is very difficult to create rules that accurately predict the best topology choice without carrying out, at least partially, the parameter selection process.

BLADES [10], uses divide and conquer solutions strategy, partitioning the circuit design in smaller tasks which are solved by subcircuit design modules. In the

topology selection part it uses Circuit topologizer, which is actually a configuration processor. It looks at the input data and tries to determine the circuit topology and the subcircuit design modules to be called. The circuit topologizer determines those factors, which influence the circuit topology, and tries to create a topology to meet these constraints. e.g., the circuit topology may be influenced by the overall gain, or output current required, as well as the input control and bias circuits will be used. Once the circuit topology is determined, the system determines the specifications of the each subcircuit building block, which in turn will determine the internal topology of each subcircuit. This step is called specification partitioning, which is not the obvious task and also not possible for every topology.

FASY [2], a design system for analog circuits, uses fuzzy logic based reasoning to select the topology among a fixed set of alternatives. Decision rules used for topology selection process are introduced by an expert designer. Selected topologies are graded on the scale of 0 to 100, indicating their relative suitability to performance specifications. The designer chooses one of them or allows FASY to choose the highest rated topology. The selected topology is given to the circuit parameter optimizer. If the final design is accepted, it is stored in the database. The experience gained with these successful designs can be used to modify the topology decision rules. Sometimes the topology decision rules cannot be acquired due to lack of experience (e.g., in case of anew technology) or due to conflicting specifications. In those cases, FASY automatically generate the decision rules by means of neuro-fuzzy techniques. For automatic rule generation specification space is clustered in an adequate number of cells, each one representing a set of user specifications. In case of n specifications, it leads to n-dimensional cells. For each cell and each possible topology, an optimization process is carried out using FASY optimizer. The final value of cost function is considered as a figure of merit of the related topology with this set of user specifications. Device sizing here is two-step process. First simple analytical equations are used to obtain a solution near the absolute minimum of the cost function. In the second phase standard gradient algorithm, which uses SPICE to compute circuit performances, is used to obtain the final design.

All the above approaches separate topology selection and parameter selection. In some cases there is fine-grained separation (e.g., OASYS) while in most other cases the separation is coarse-grained. Some recent papers use approaches, which eliminates this separation; i.e., simultaneous topology selection and parameter

selection. A new approach to cell-level analog circuit synthesis is presented in [3]. This approach formulates analog synthesis as a Mixed-integer Nonlinear Programming (MINLP) problem in order to allow simultaneous topology selection and parameter selection. Topology choices are represented as binary integer variables and design parameters (e.g., device sizes and bias voltages) continuous variables. A supercircuit is formulated, from which all topologies can be derived just by inclusion or exclusion of some subcircuits. Equations are derived for various performance parameters in terms of design variables, which in this case are device sizes and bias voltages. Using the performance equations, constrained optimization problem is formulated. Branch and Bound algorithm is used to solve the MINLP problem. If there are n binary variables then topology choices are 2^n. To improve the speed infeasible topologies are removed by inserting linear constraints. This approach gives results, which are comparable to exhaustive search for a wide range of specifications. This approach is more like topology creation process rather than topology selection process.

1.4 OBJECTIVE

The Main objective of our work is to propose a well-defined methodology to select a topology among the pool of available topologies, which fulfills user specifications. The Second objective is to help the user in modification of specification if none of the topologies satisfy the user requirements.

In the present work the methodology adopted for 'topology selection of analog circuits' combines the advantages of both the optimization-based and knowledge based approaches. Topology definition is quantitative while retaining all the features of behavioral description. This makes our study based more on analytical equations and constraints while avoiding heuristics, which used to appear much frequently in the earlier approaches. Genetic algorithm based optimization approach is adopted, which provide equally good results in comparison to recent work done towards the same problem employing fuzzy logic approach.

The organization of the thesis is as follows.

Chapter 2 describes the overview of the methodology adopted in this work, e.g., formulation of the problem, the concept of genetic algorithm, objective function formulation, and the algorithm used to solve the optimization problem.

Chapter 3 presents the application of the proposed approach, first to topology selection of MOS current sources and then to topology selection of CMOS op-amps. The type of op-amps considered in this work are a simple CMOS operational transconductance amplifier (OTA), the Miller-compensated CMOS OTA, the folded cascode CMOS OTA.

The summary and conclusion along with the scope for future work are discussed in Chapter 4.

CHAPTER 2

Topology Selection Methodology - An Overview

2.1 Introduction

This chapter describes the topology selection approach developed in the present work for cell level analog circuits. It is based on a new description of topology as a set of constraints among the specifications. An optimization technique is used to select the topologies on the basis of this definition.

Figure 2.1 depicts schematically the major steps in analog circuit design. For automation of analog design processes all three steps namely topology selection or generation, parametric optimization and Layout generation have to be automated. As mentioned earlier in the introduction, most of the work in analog CAD has been devoted to the area of parameter optimization.

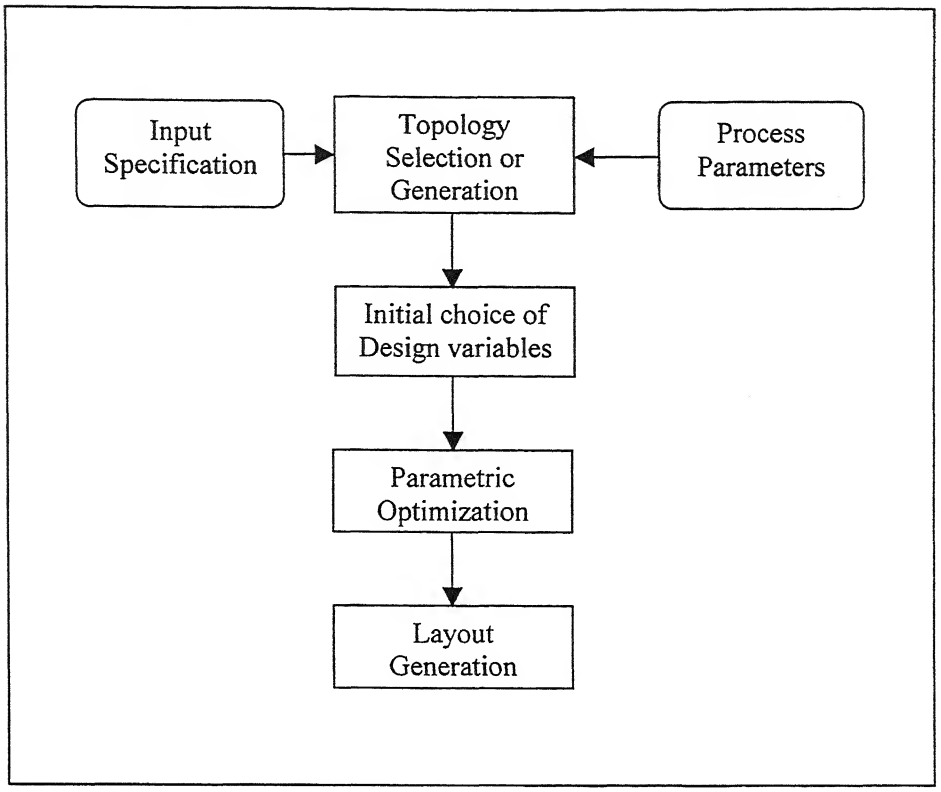


Fig 2.1–Procedure for analog circuit design

However, topology selection, although very important, has attracted less attention. To date proposed topology selection strategies have relied on a limited set of approaches, which can be classified as shown in the table below.

Table 2.1 Classification of different topology selection approaches

	Topology Generation	Topology Selection
Qualitative or heuristics based	OPASYN [13]	FASY[2] STAIC [5] OASYS [4]
Quantitative Approach	IPTS [3]*	PRESENT WORK

* *Integer programming based topology selection of cell-level analog circuits*

It can be seen that most of approaches for topology selection reported till now are of the type "topology selection/generation based either on qualitative statements or heuristics". A few them search exhaustively through all available topologies, or alternate iteratively between topology selection and parameter optimization steps for various portions of the circuit. Only a single approach uses quantitative basis, but that

is also applied for topology generation. Till date none of the existing approaches have claimed to select topology on the basis of pure quantitative descriptions of a topology. It is obvious that topology selection is intimately tied to how a topology is defined. Different descriptions of topology would result in different approaches to its classifications. This approach is further elaborated in the next section.

2.2 Topology Description

2.2.1 Introduction

To carry out topology selection, the following requirements must be met.

1. Each topology needs to be described in such a manner that it is easy to distinguish it from other alternative topologies.
2. The specifications or some function of them must be used as the topology selection criterion.
3. The selection criterion chosen above must be related to the topology description in a simple and explicit manner.

The first statement is obviously true. In order to select one member of the group, we have to distinguish it in some manner from the other members present. The second requirement is forced by the fact that topology selection is being carried out to find the topology that must be capable of satisfying the specifications. The need for third requirement can be illustrated with the following example. Suppose a topology is described by its circuit schematic. This description, being unique, satisfies the first condition and let us takes the specifications themselves as the selection criterion to satisfy the second condition. However, a circuit schematic by itself is very difficult to use for carrying out topology selection because the third condition is not met. The relationship between a schematic and the specifications is neither simple nor explicit but can only be extracted through a detailed procedure, which would practically amount to an attempt to design the topology itself. If test of suitability of topology for a given set of specifications takes the same time or effort as the design itself then the purpose of topology selection as an activity prior to detailed design is defeated. The whole idea of topology selection rests on the need to select a topology without designing it.

Besides its schematic diagram, a topology is often characterized by qualitative statements, which highlight its unique strengths/weaknesses. For example, a statement like " It offers high gain but low input resistance" is often used to characterize a common base amplifier or a statement like "It offers high output resistance" is used with the cascode current mirror. Such a description of topology can and has been used widely in the topology selection methods reported till date. To select the topology on the basis of such qualitative statementsm, some numerical value have to attached to terms like high, low etc. For example a statement like "*IF output resistance required is large ($\geq 1M\Omega$) THEN use cascode current mirror. IF output voltage required is less (≤ 0.5 V) THEN suitability of simple current mirror topology is large.*" can be used as criterion for selection of current mirrors. However, this method of topology selection suffers from the problem of being fuzzy and impercise. These two topology selection schemes described above form two ends of topology selection methodologies as illustrated in Fig.2.2

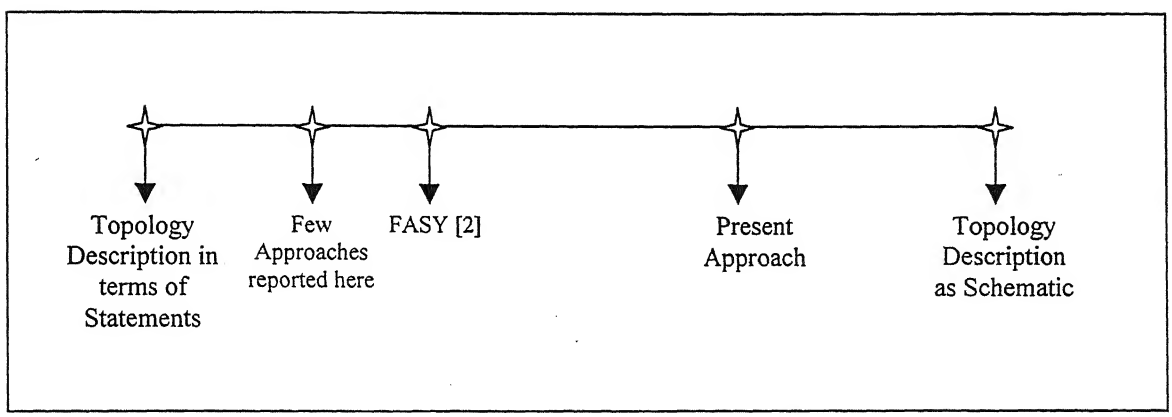


Fig 2.2 Classification of different approaches of topolgy selection based on performance.

The first method of describing topology as a schematic results in a selection method, which is very precise but is imprctical because it is very time consuming. The second method is very simple but impercise. To overcome some of the disadvantages of the second approach, use of fuzzy logic for topology selection has been proposed. Fuzzy logic has been specially proposed to deal with uncertain information and it provides an effective means of capturing the approximate inexact nature of human reasoning. But sometimes the topology decision rules cannot be acquired in terms of linguistic terms due to lack of experience in the case of new technology or due to the existence

of conflicting performance requirements. These rules defined by an expert are in such a way that suitability of any topology for the particular specifications, is small, medium, large or very large. But these rules do not define a well-defined line, which can discriminate between large and very large. If suitability of one topology for particular specification is large, then how much large. A more sophisticated topology selection method would therefore be necessary. For this, there is a strong need to define topology more precisely and in a technology independent manner that formulates problem of measuring topology adequacy efficiently and at the same time it should retain all the information about its behavior.

2.3.2 New Description

In the present work, a topology is characterized by a set of equations, which describe the constraints among the specifications. The logic for this description can be understood using Fig. 2.3. All the information, which is traditionally described in terms of statements, is embedded in these constraints. In order to illustrate this point let us take two topologies of current mirror, one simple current mirror and the other cascode current mirror. Conventionally, these two topologies can be characterized by the following set of statements.

For simple current mirror:

"Simple mirror offer moderate output resistance and lowest output voltage."

For cascode current mirror:

"Cascode current mirror offers higher output resistance for a given current."

If such a definition is to be used for selection of topology then a definite numerical value has to be attached to terms like high, low, medium etc. However this number is highly technology dependent. The description of simple current mirror and cascode current mirror in terms of equations is shown in third column of the table 2.2.

Table 2.2 comparison between conventional and present description of topology.

Topology Name	Conventional Description	Alternative Description
Simple Current Mirror	Simple mirror offer moderate output resistance and lowest output voltage	$R_{os} = \frac{1+\lambda_n V_{os}}{\lambda_n I_{os}}$ $V_{os} = \Delta V$
Cascode Current Mirror	Cascode current mirror offers higher output resistance for a given current	$R_{oc} = \left[\frac{1+\lambda_n(\Delta V + V_{tno})}{\lambda_n I_{oc}}\left(1+\frac{2(1+\lambda_n \Delta V)}{\lambda_n(\Delta V + V_{tno})}+\frac{1+\lambda_n \Delta V}{\lambda_n I_{oc}}\right)\right]$ $V_{oc} = 2\Delta V + V_{tno}$

Defintions of symbols used in table 2.2 are as follow.

R_{os} – Output resistance of simple current mirror.

R_{oc} – Output resistance of cascode current mirror.

V_{oc} – Min. output voltage below which output transistor goes into linear region in cascode current mirror.

V_{os} – Min. output voltage below which output transistor goes into linear region in simple current mirror.

V_{tno} – Threshold voltage for NMOS transistor at zero body-source voltage.

I_{os} – Output Current of simple current mirror.

I_{oc} – Output Current for cascode current mirror.

ΔV – Gate overdrive.

These constraints were derived from symbolic analysis of the circuits and are described in deatil in chaper 3. It can be shown that the second description encompasses within it all the information, which is there in the first description. By careful inspection of constraints it is obvious that R_{oc} is large as compare to R_{os} for same value of V_o and I_o. Also, for same value of I_o and R_o, simple current mirror ceases to work at lower V_o as compare to cascode current mirror. For example, for 10 μA current, it is feasible to obtain R_o of 35 MΩ in cascode current mirror while with a

simple current mirror R_o of only 3.8 MΩ is possible. This is consistent with what is usually described as an advantage of cascode current mirror and a limitation of simple current mirror. Consider another example where for 1 μA current and R_o of 5 MΩ it is feasible to obtain 0.31 V in simple current mirror while with cascode current mirror minimum output voltage can not be less than 1.57 V. This confirms what is described in column 2 of table 2.2. Therefore, while new description includes within it all the information that is traditionally presented in the form of qualitative statements, it also offers the advantage of being precise. In the present approach exact information about the adequacy of the topology is available in terms of numbers as shown by above two examples. Another advantage of the presenr approach is that technology dependent parameters are represented symbolicaly and can by easily modified.

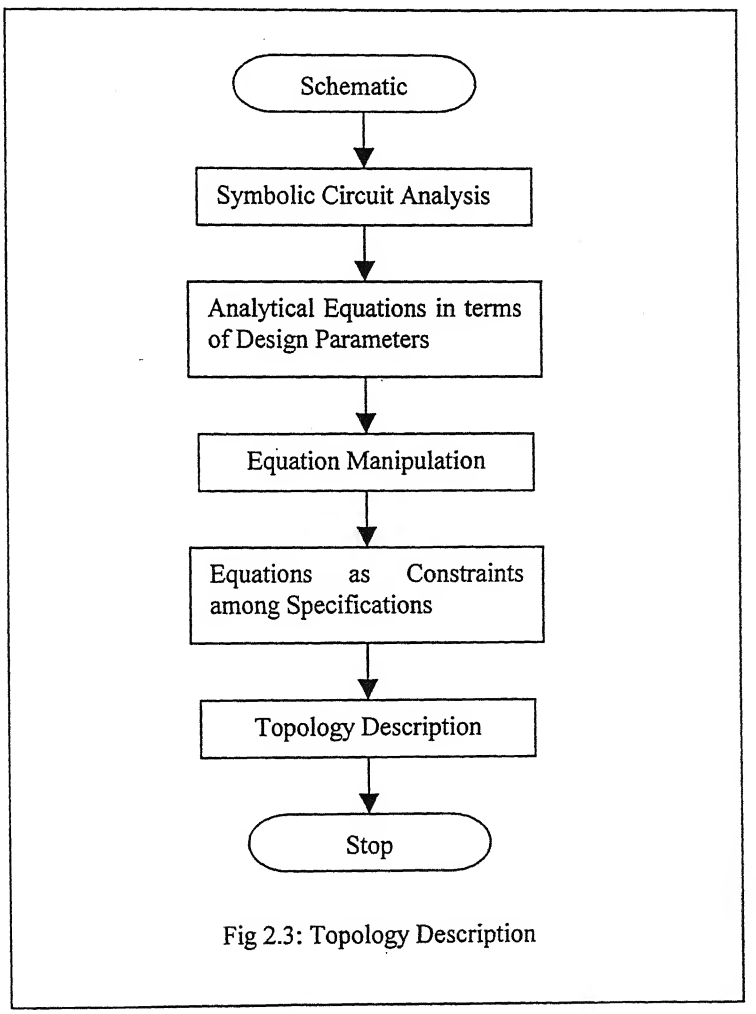


Fig 2.3: Topology Description

To describe topology in terms of relationships among the specifications, small signal analysis of all the topologies have carried out to obtain the equations, which describe the dependence of each specification on design parameters such as transistor sizes and simplified device model parameters like threshold voltage and other technology parameters. Although analysis is often time consuming and not stright forward, they are available in litrature to some extent. Further, symbolic analysis simulator can be used to generate performance equations. IDAC [12] has attempted to generate the analysis equations with the help of symbolic analysis. A recent approach, somewhere between the equation-based and simulation-based approaches is ASTRX/OBLX [24]. ASTRX/OBLX uses an extremely efficient method to automatically determine the all small-signal performance measures automatically, thus eliminating the effort required to create equations for predicting performance. These equations are then formulated as relationship amongst specifications. This describes topology in terms of constraints, which are the relations amongst specifications and process parameters. For op-amps, equations are derived for various performance parameters like gain, bandwidth, phase margin, slew rate, power dissipation, noise and area in terms of transistor sizes and process parameters. e.g., in terms of device transconductance's (gm's, gd's) and currents(id's). Parameters, which are internal to topology, are removed one by one from these equations. In the end of this process, we get relationships among the specification and process parameters [3].

2.3 Topology selection

Once a topology is defined in terms of constraints, the first criterion for selecting a topology is satisfaction of these constraints. On this basis topologies can be clssified into two sets S_1 and S_2. One set (S_1) contains topologies, which satisfy the constraints, and other set (S_2) contains topologies for which constraints are violated. For the cases where set S_1 contains only one element, we choose that topology irrespective of any other criteria. If S_1 contains more than one element than there is need to have a selection criterion to find out the most suitable topology among available choices. In the present approach this is done on the basis of area but a different criteria can also be specified by the user. In the present definition of topology, most of the constraints are of equality type. So in most of the cases, set S_1 often contains no element,

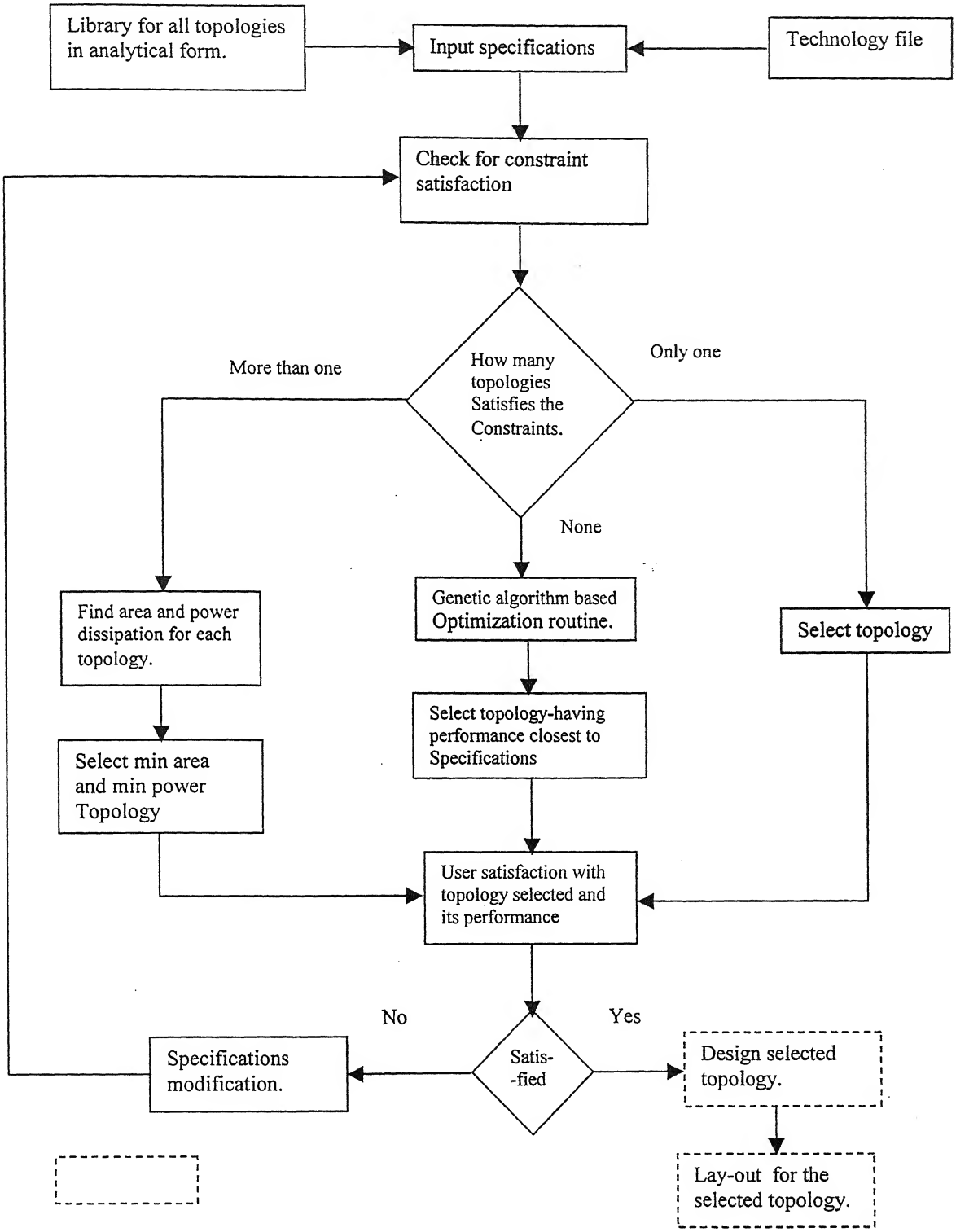


Fig. 2.4. Flow chart for the topology selection flow

meaning no topology satisfies the constraints. In this case, it has to be determined as how close the performance of a topology to the specifications while obeying all the constraints (within a pre-specified error). On the basis of the capability of a topology to satisfy constraints and total error between performances and specifications, topologies are ranked. To carry out all the above stated processes, an optimization technique has to be applied. After optimizing for each topology, the first step is to find out error between user given specification and performance parameters. Topologies, for which errors are less than tolerance, are stored in set S_1, which then set serves as topology library for further selection. Topologies for which error is greater than the tolerances are stored in set S_2. If S1 contains more then one element than minimum area as mentioned earlier is used as selection criterion. If set S1 is null, it means that no topology is able to satisfy the specifications provided by the user. In this case, a modification in specifications becomes necessary to proceed with the design.

2.4 Optimization

Many methods of optimization are available like Steepest descent method, Penalty method, Powel conjugate method and other gradient-based methods, but most of them suffer from the problem of local minimum. Due to complex dependencies between specifications and circuit performance, only statistical method like simulated annealing, genetic algorithm are suitable because of their greater immunity against the problem of local minimum.

2.4.1 Genetic Algorithm

Genetic algorithm (GA) is computerized search and optimization algorithm based on the mechanics of natural genetics and natural selection. GA mimics the survival of fittest principle of nature to make a search process. Therefore GA's are naturally suitable for maximization type problem. Present problem is of minimization type, but it is converted into maximization type. In general, fitness function is first derived from the objective function and used in successive genetic

operations. The operation of GA begins with a population of random strings representing design or decision variables. Each string is evaluated to find the fitness value. The population is then operated by three main operators'– reproduction, crossover and mutation–to create new population of points. The new population is again evaluated and tested for termination. If the termination criteria are not met, the population is iteratively operated by the above three operators and evaluated. The procedure is continued until the termination criterion is not met. One cycle of these operations and the evaluation procedure is known as a generation in GA's terminology. More information about genetic algorithm and literature can be found in the appendices or refer [48]. In present problem real coded genetic algorithm is applied [49].

2.4.2 Problem Formulation

We perform circuit selection using constraint optimization formulation, but solved in unconstrained fashion. In the present approach, the optimization problem is formulated as the minimization type, which is solved using real coded genetic algorithm (RGA).

$$f_{obj} = w_i \sum_{i=1}^{Nesp} \left(Error_i\right)^2 \tag{2.1}$$

$$Error_i = \left(\frac{P(x)}{Pspec} - 1\right) \tag{2.2}$$

$$\text{subjected to g(x)} \begin{matrix} \{g(x) \geq 0\} \\ \{h(x) = 0\} \end{matrix} \tag{2.3}$$

where

Nesp = No. of specifications.

$Pspec_i$ = Performance specification given by the user.

f_{obj} = Objective function to be minimized.

P(x) = Performance related to other specifications.

$g(x), h(x)$ = constraints which define topology.

Error_i = Error between user specifications and performance parameters which satisfy the constraints.

w_i = weight assigned to i'th specification.

To allow the use of genetic algorithm, we perform the standard conversion of this constrained optimization problem to an unconstrained optimization problem with the use of scalar weights. As a result goal becomes the minimization of a scalar cost function, C(x), defined by

$$C(x) = \sum_{l=1}^{Nesp} f_{obj}(x) + \sum_{i=1}^{k} r_i * gi(x) + \sum_{j=1}^{t} rj * h_j(x) \qquad (2.4)$$

r_i, r_j = weight assigned to constraints.

k = number of inequality constraints.

t = number of equality constraints.

The key to this formulation is that the minimum of C(x) corresponds to the topology that best matches the given specifications. Thus synthesis task cultivates into two more concrete tasks: 1) Evaluating C(x) and 2) Searching for its minimum. However performing these tasks is not easy. In equation based–synthesis tools, evaluating C(x) is done using designer supplied equations. In present case C(x) is evaluated with the help of equations, which describe topology. After optimizing for each topology the first step is to find out error between user given specification and performance parameters. Topologies, for which errors are less then tolerance, are stored in set S1. Set S1 serves as topology library for further selection. Topologies for which error is greater than tolerances are stored in set S2. For the cases, where set S1 contains only one element, we choose that topology irrespective of any other criteria. If S1 contains more then one element than there is need to have a selection criterion to find out the

suitable topology among available choices. In the present approach topology selection is done on the basis of area but a different criteria can also be used specified by the user.

2.5 Specification modification

In some cases even after optimization there will be error in satisfying constraints, which will considerably be larger than tolerances provided. If Set S_1 contains no element, it means that no topology is able to satisfy the specifications provided by the user. Therfore modification in specifications becomes necessary to proceed further with the design process. To modify the specification it is assumed that the user has some knowledge of the circuit topologies and approximate values of performance specifications achieved by it. The present description of a topology in terms of constraints among the specifications is very useful for specification modification also. It gives in a concise form, the various relationships among the specifications, therby allowing the designer to suitabily modify them.

DEPARTMENT OF ELECTRICAL ENGINEERING
IIT-KANPUR

M.Tech Thesis Defence

Mr. Arun K. Sharma (Roll no: 9810406) will defend his M.Tech Thesis titled "**A New Approach for Topology Selection of Analog Circuits**" on 17-03-2000.

Date: 17-03-2000
Time: 3.00 p.m.

Venue: ACES DA-229

All intrested are welcome

Thesis Supervisor
Dr. Baquer Mazhari

CHAPTER 3

Implementation and Results

3.1 Introduction

The validity of topology selection approach as described in chapter 2 is demonstrated here. This chapter describes the results for selection of two classes of circuits, namely current mirrors and operational amplifier.

3.2 Current Mirrors

The current mirror, also known as current source/sink, is a basic building block that is widely used in analog circuit design. Ideally, the output impedance of a current source/sink should be infinite and capable of drawing/supplying a constant current over a wide range of voltages. However, finite values of output impedance, and a limited output swing due to the need of keeping device in saturation ultimately limit the performance of the mirror. For the current mirrors, the objective is to obtain a large output resistance for a given current, a minimum output voltage not greater than the limit specified by designer, and minimize area.

Depending upon the specifications one of the following mirrors can be used.

1. Simple current mirror
2. Cascode current mirror.
3. Wilson current mirror.

Table 3.1 shows performance specifications, which forms the basis for selection of current mirror in our experiments.

Table 3.1

Sl. No	*Symbol*	*Specification*	*Typical objective*
1	I_{out}	Output current	User specified
2	V_{outmin}	Minimum Output voltage	Minimize
3	R_{out}	Output resistance	Maximize
4	*AREA*	Active area	Minimize

3.2.1 Simple Current Mirror

The schematic of a simple current mirror is shown in the Fig.3.1.The mathematical equations that relate the performance specifications to the different device characteristics are given below. It is assumed throughout that the transistors M1 and M2 are of same width (W) and length (L). The bias current (I_{bias}) is equal to the output current (I_{out}).

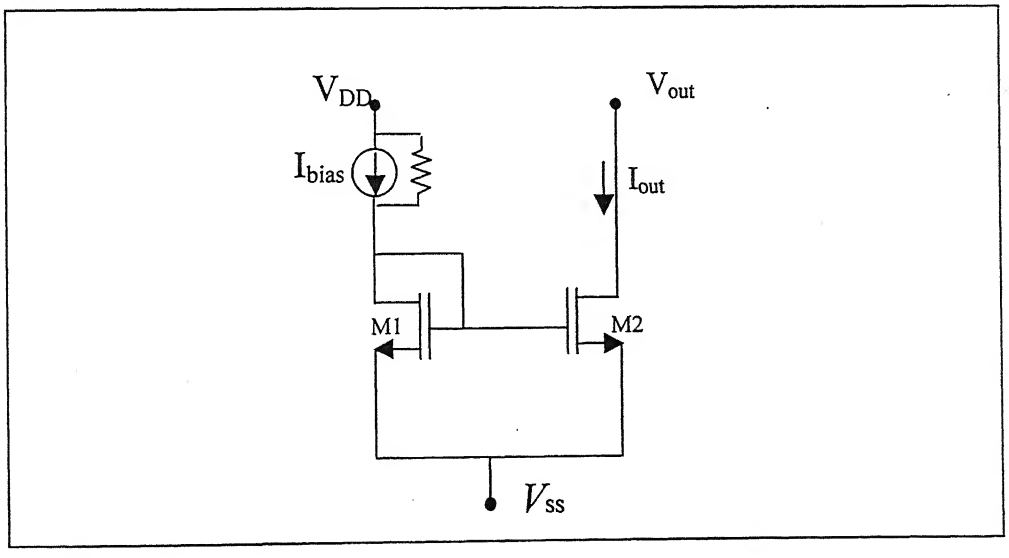


Fig 3.1 Schematic of a Simple current mirror

The output resistance (R_{os}) is given by,

$$Ros = r_{o2} = \frac{1 + \lambda Vds_2}{\lambda Ids_2} \tag{3.1}$$

where I_{ds2} is the drain to source current of M2 and equal to output current (I_{os}), V_{ds2} is the drain to source voltage of M2 and equal to output voltage(V_{os}).
The minimum output voltage (Voutmin) is given by,

$$V_{os} = V_{out\,\min} = V_{GS2} - V_{tno} \tag{3.2}$$

The active area taken by the current mirror is,

$$AREA = 2 \times W \times L \tag{3.3}$$

The equations listed above are manipulated to obtain a set of equations that describe relationships among the specifications.

$$R_{os} = \frac{1 + \lambda_n V_{os}}{\lambda_n I_{os}}$$

$$V_{os} = \Delta V$$

R_{os} – Output resistance of simple current mirror.
V_{tno}– Threshold voltage for NMOS transistor at zero body-source voltage.
I_{os} – Output Current of simple current mirror.
V_{os}– Min. output voltage below which output transistor of simple current mirror goes into linear region.
ΔV – Gate overdrive $=V_{GS} - V_{tno}$.
These equations describe the essence of a simple current mirror topology.

3.2.2. Cascode Current Mirror

The cascode current mirror is a combination of two simple current mirrors. This configuration is used to increase the output resistance of a current source.

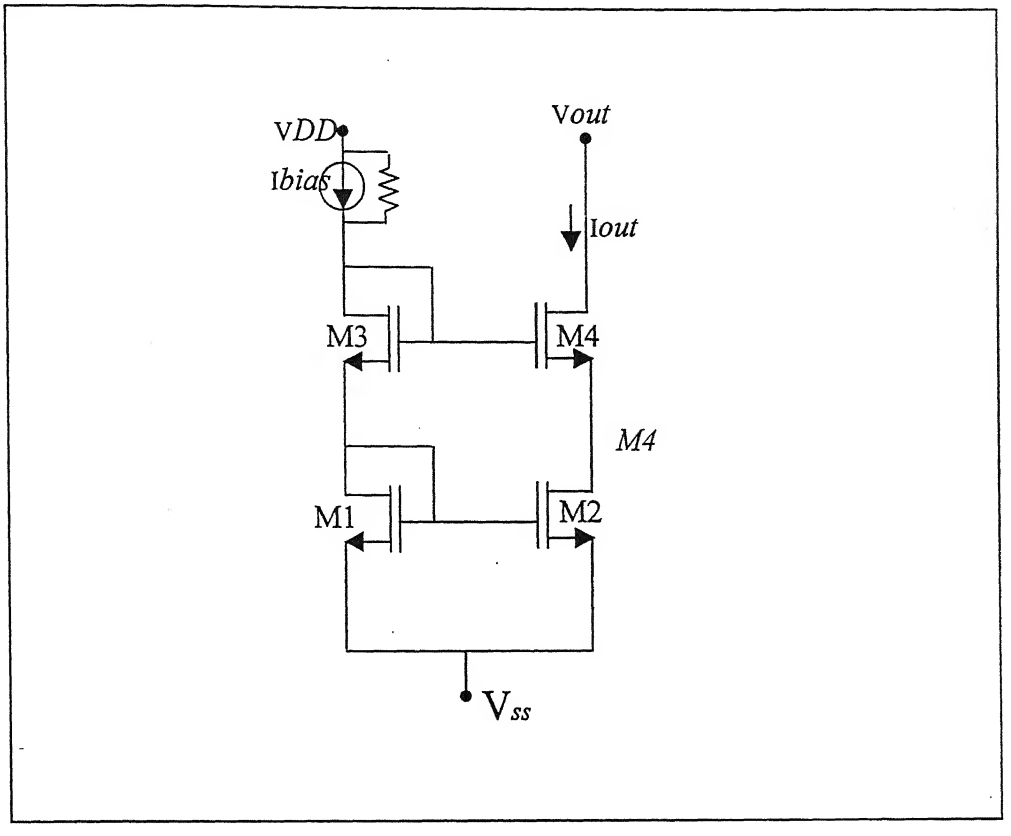


Fig. 3.2: Schematic of a Cascode current mirror.

The schematic of a cascode current mirror is shown in the Fig.3.2. The mathematical equations that relate the performance specifications to the different device characteristics are given below.

The output resistance (Rout) of the current source is given by [36].

$$Roc = r_{o2}\left(1+\left(g_{m4}+g_{mb4}\right)r_{o4}\right)+r_{o4} \qquad (3.4)$$

where r_{o2} and r_{o4} are the drain to source resistances of M2 and M4, g_{m4} and g_{mb4} transconductance and gate-body transconducatnce of transistor M4.

The minimum output voltage (V_{outmin}) is given by

$$V_{oc} = V_{out\min} = V_{GS2} + V_{GS4} - V_{tn4} \tag{3.5}$$

where V_{GS2} and V_{GS4} are gate source voltage of M2 and M4 respectively, and V_{tn4} the threshold voltage of M4 with body effect.

The active area taken up by the current source is given by

$$AREA = (W_1 + W_2 + W_3 + W_4) \times L_{\min} \tag{3.6}$$

where W_i are the width of i^{th} transistor and L_{min} is the minimum length of the transistor.

Based on the above assumptions and equations, cascode current mirror topology can be described as following constraints.

$$Roc = \frac{1 + \lambda_n(\Delta V + Vtno)}{\lambda_n Ioc}\left(1 + \frac{2(1 + \lambda_n \Delta V)}{\lambda_n(\Delta V + Vtno)} + \frac{1 + \lambda_n \Delta V}{\lambda_n Ioc}\right)$$

$$V_{oc} = 2\Delta V + V_{tno}$$

R_{oc} – Output resistance of simple current mirror.

I_{oc} – Output Current of simple current mirror.

V_{oc} – Min. output voltage for below which output transistor of cascode current mirror goes into linear region.

3.2.3. Wilson Current Mirror

The basic current mirror is improved significantly with negative feedback. Wilson's current mirror uses this concept to offer stable current values for wide voltage swings and enhanced output resistance. The mathematical equations that relate the performance specifications to the different device characteristics are given

below. The current source (I_{bias}) is chosen to be equal to the desired output current. The transistors M1, M2, M3 are taken to be of same dimensions.

The output resistance (R_{ow}) is given by,

$$R_{ow} = r_{o3}\left(1 + g_{m2}(r_{o1} \parallel r_{o2}) + g_{mb3}\left(\frac{1}{g_{m3}}\right) + \frac{1}{r_{o3}g_{m3}}\right) \qquad (3.7)$$

where r_{o1}, r_{o2} and r_{o3} are the drain-source resistances of transistors M1, M2, and M3 and g_{m2}, g_{m3}, g_{mb3} are conductances of M2, M3 respectively . g_{mb3} is the gate-body transconductance of transistor M3.

The minimum output voltage (V_{ow}) is given by,

$$V_{ow} = V_{GS3} + V_{DS4,sat} = V_{GS3} + V_{GS4} - V_{tn4} \qquad (3.8)$$

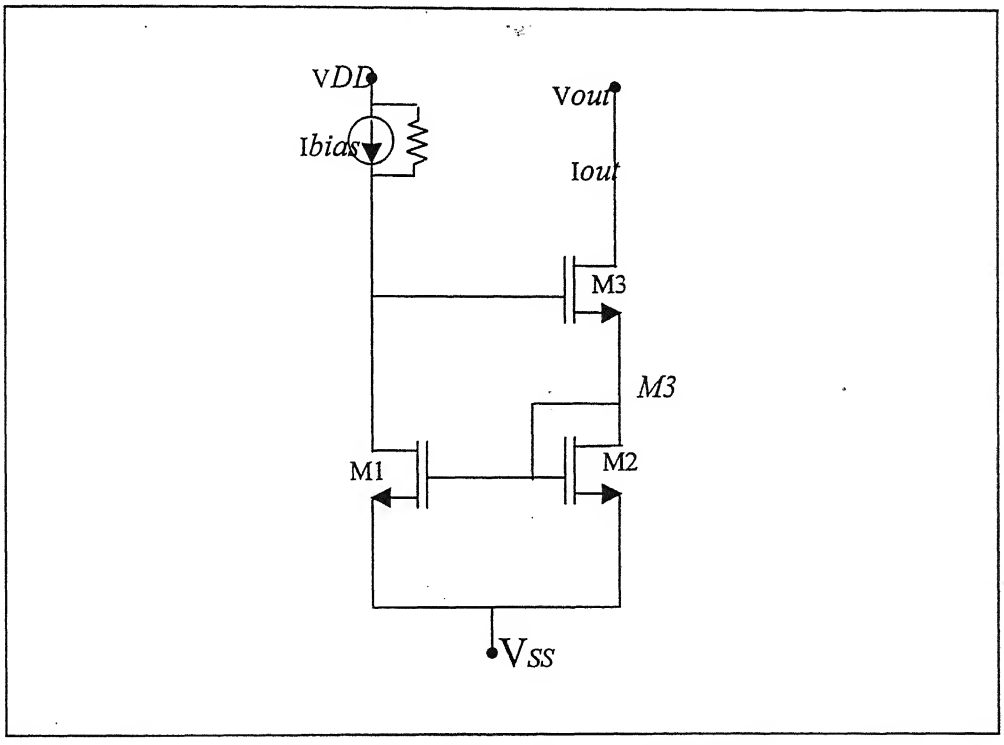


Fig. 3.3: Schematic of Wilson current mirror.

The active area taken up by the current source is given by

$$AREA = (W_1 + W_2 + W_3) \times L_{min} \qquad (3.9)$$

Based on the above assumptions and equations, Wilson current mirror topology can be described by the following constraints.

$$R_{ow} = \frac{1+\lambda_n \Delta V}{\lambda_n I_{ow}} \left(1 + \frac{2(1+\lambda_n \Delta V)}{\lambda_n \Delta V} + \frac{\lambda_n \Delta V}{1+\lambda_n \Delta V} \right)$$

$$V_{ow} = 2\Delta V + V_{tno}$$

R_{ow} – Output resistance of wilson current mirror.

I_{ow} – Output Current of wilson current mirror.

V_{ow} – Min. output voltage for below which output transistor of wilson current mirror goes into linear region.

3.3 Results for Current Mirrors

Several experiments were performed with the program written to select one topology among three topologies described earlier. All the experiments are carried out for 3μm technology, process parameters for which are described in appendix-II.

Experiment No. 1.

Table 3.3

Specification Name	Specification	Simple current Mirror	Cascode current Mirror	Wilson Current Mirror
Output Resistance(MΩ)	10.00000	3.845278	15.364272	24.732796
Output Voltage(V)	1.500000	0.578748	1.351949	1.397171
Output Current(μA)	10.00000	12.440908	10.08453	14.499306
Active Area(μm2)	75.0000	30.315788	55.550675	43.028504
%age Error	——	25.000000	2.4711325	11.248265
Topology Selected	CASCODE CURRENT MIRROR			

Experiment No.2

Table 3.3

Specification Name	Specification	Simple current Mirror	Cascode current Mirror	Wilson Current Mirror
Output Resistance(MΩ)	10.00000	3.114670	5.615238	15.364272
Output Voltage(V)	2.000000	2.112294	1.300317	1.351950
Output Current(μA)	20.00000	15.487487	17.629547	21.421802
Active Area(μm2)	100.0000	56.631578	107.101349	82.057007
%age Error	——	3.7869778	0.5820728	0.12634505
Topology Selected	WILSON CURRENT MIRROR			

Experiment No.3.

Table 3.4

Specification Name	Specification	Simple current Mirror	Cascode current Mirror	Wilson Current Mirror
Output Resistance(MΩ)	5.000000	46.450954	89.418928	85.628580
Output Voltage(V)	0.250000	0.362896	1.228493	1.022653
Output Current(μA)	1.000000	1.027173	1.513615	1.564844
Active Area(μm2)	75.0000	55.098243	59.155068	57.902850
%age Error	——	5.098243	382.979584	238.797348
Topology Selected	SIMPLE CURRENT MIRROR			

Following observations can be made on the basis of results shown above.

- For moderate output resistance (<5MΩ) and low minimum output voltage (<0.5V) simple current mirror is a better choice as compared to other alternatives as it requires minimum area while satisfying all the specifications.

- For large output resistance (>10MΩ) cascode current mirror is a better choice. Although simple current mirror requires less area, it doesn't meet the specification of output resistance.

These two observations are in the agreement with what is commonly known about these current mirrors. In order to further verify the correctness of the topology selection approach described here, full design for each of the topologies was carried out. Initial design was done using analytical equations and then optimization was done using Microsim PSPICE Optimizer [50]. Table 3.5-3.7 shows the results obtained after design of each of the topologies for the specifications shown earlier. It can be seen that results for topology selection using present approach are in agreement with that of selecting topology after carrying out full design. The diffrence in numerical values, one obtained in the present approach and other from microsim pspice optimizer is mainly due to approximate analytical equations.

Experiment No.4

Table 3.5

Specification Name	Specification	Simple current Mirror	Cascode current Mirror	Wilson Current Mirror
Output Resistance(MΩ)	10.00000	5.4034	18.937106	10.3347
Output Voltage(V)	1.500000	0.8203	1.4053	1.345
Output Current(μA)	10.00000	10.6408	10.00000	9.8239
Active Area(μm2)	75.0000	28.3033916	54.669714	114.722649
%age Error	——	52.8813	0.0000000	52.963532
Topology Selected	CASCODE CURRENT MIRROR			

Experiment No.5

Table 3.6

Specification Name	Specification	Simple current Mirror	Cascode current Mirror	Wilson Current Mirror
Output Resistance(MΩ)	10.00000	2.71384	2.77690	45.678
Output Voltage(V)	2.000000	0.410491	1.69000	1.26357
Output Current(μA)	20.00000	21.4406	20.0000	19.9737
Active Area(μm2)	100.0000	97.8548992	54.669714	90.8103504
%age Error	——	7.28616	7.2231	0.1315
Topology Selected	WILSON CURRENT MIRROR			

Experiment No. 6

Table 3.7

Specification Name	Specification	Simple current Mirror	Cascode current Mirror	Wilson Current Mirror
Output Resistance(MΩ)	5.000000	53.86	99.66	91.02
Output Voltage(V)	0.250000	0.341034	1.40563	1.31
Output Current(μA)	1.000000	1.01374	1.00165	0.98161
Active Area(μm2)	75.0000	68.94	82.58	91.495824
%age Error	——	3.641360.	474.947	453.769
Topology Selected	SIMPLE CURRENT MIRROR			

3.4 Operational Amplifiers

Operational amplifier (op-amp) is a basic building block used in wide variety of analog circuits, e.g., A/D converters, switched capacitor filters, etc. Therefore the topology selection of op-amp is of tremendous importance in order to meet performance specifications for circuits of larger complexity. The topology selection

procedure described here chooses one topology from a set of three alternatives namely: Simple operational transconductance amplifier (OTA), the basic two-stage (BTS) op-amp and the folded cascode op-amp.

The set of performance specifications for which the program is written are tabulated in Table 3.8. It must be noted that depending upon the objective (to minimize/maximize or to have a desired value) chosen by the user, the function for that performance specification is suitably manipulated.

Table 3.8 The performance specifications and objectives, which forms basis for selection of op-amp in present experiments.

Table 3.8

Sl. No	Symbol	Performance specification	Typical objective
1	Gain	*Voltage gain of the amplifier*	*Maximize*
2	UGF	*Unity gain frequency*	*Maximize*
3	PM	*Phase margin*	*User specified*
4	SR	*Slew rate*	*User specified*
5	PD	*Power dissipation*	*Minimize*
6	AREA	*Active area*	*Minimize*
7	CL	*Output capacitance*	*User specified*

3.4.1 Simple Operational Transconductance Amplifier

The schematic of a simple OTA is shown in Fig. 3.4. This is one of the simplest, widely versatile MOS op-amp with moderate gain and used in a variety of applications driving on chip load where minimum area is a desirable aspect.

The mathematical equations that relate the performance specifications to the different device characteristics are given below.

1. Gain

The gain of OTA is given by [36]

$$Gain = g_{m1}\left(r_{o1} \parallel r_{o4}\right), \tag{3.10}$$

Where g_{m1} is the transconductance of M1, r_{o1} and r_{o2} are the drain-source resistances of M2 and M4 respectively.

2. *Unity-gain frequency (UGF)*

The unity-gain frequency of OTA is given by [36]

$$UGF = \frac{g_{m1}}{2\pi(C_L + C_{n2})}, \tag{3.11}$$

where C_L is the load capacitance, and C_{n2} is the capacitance at node 2 due to transistor parasitic at node 2.

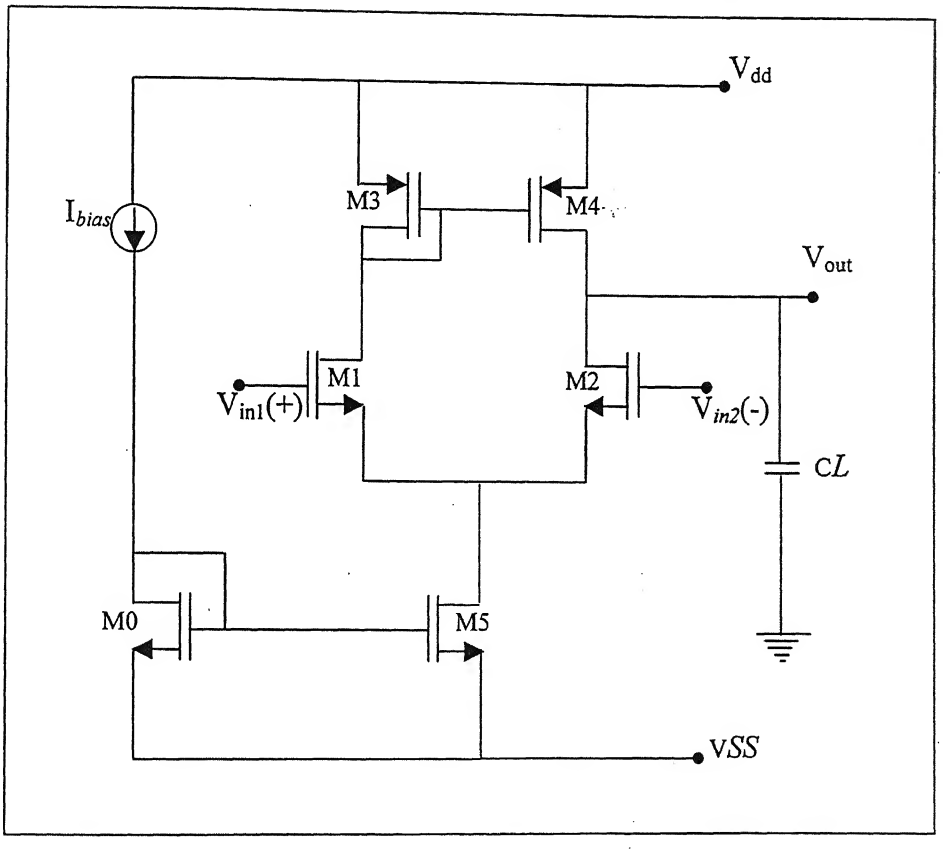


Fig.3.4: Schematic of a simple operational transconductance amplifier

3. *Phase margin(PM)*

The phase margin is given by the following expression.

$$PM = 90^\circ - \tan^{-1}\left(\frac{UGF}{f_{nd}}\right), \tag{3.12}$$

where f_{nd} is the non-dominant pole created at the node 1 given by

$$= \frac{1}{2\pi R_{n1} C_{n1}}, \tag{3.13}$$

where R_{n1} ($\approx 1/g_{m3} = 1/g_{m4}$) is the resistance at the node 1, g_{m3} and g_{m4} are the transconductance of M3 and M4 respectively, and C_{n1} is the capacitance at the node 1 due parasitic of transistors connected to it.

4. *Slew Rate(SR)*

The slew rate is given by

$$SR = \frac{I_{d5}}{(C_L + C_{n2})}, \tag{3.14}$$

where I_{d5} is the DC current through M5, which is not equal to I_{bias}, due to the greater drain-source voltage across M5 than that across M0.

5. *Power Dissipation*

Power dissipation (PD) is given by

$$PD = (V_{DD} - V_{SS}) \times (I_{bias} + I_{d5}) \tag{3.15}$$

6. *Noise*

Each transistor contributes white noise and $1/f$ noise. The equivalent rms input noise voltage of a MOS transistor at any frequency is given by [36].

$$\overline{dv^2{}_n(f)} = \frac{8kT}{3}\frac{1}{g_m}df + \frac{K_F}{WL}\frac{df}{f}, \tag{3.16}$$

where $K_F = KF_F/C'^2_{ox}$, with KF_F being a technology parameter. In order to calculate the noise performance at low frequencies, all the capacitances are omitted. The different noise voltage sources present in an individual transistor can be clubbed together to an equivalent input noise voltage source $\overline{(dv^2{}_{nie})}$ by using the following expression.

$$\overline{dv^2_{nie}} = \sum_{i=1}^{n} \overline{dv^2_{ni}} \left(\frac{A_{vni}}{A_{vo}} \right)^2, \tag{3.17}$$

Where dv^2_{nie} is the equivalent noise of the i^{th} transistor referred to the input, A_{vni} is the gain of the i^{th} transistor from its input to the output, and A_{vo} is the overall gain of the circuit. It is observed that the noise due to M1, M2, M3 and M4 dominate the equivalent input noise. Thus it can be approximately given by the following expression.

$$\overline{dv^2_{nie}} \approx 2\left[\overline{dv^2_{n1}} + \overline{dv^2_{n3}} \left(\frac{g_{m3}}{g_{m1}} \right)^2 \right] \tag{3.18}$$

7. *Area*

The total area is taken to be equal to the sum of the active areas taken by the individual transistors, and is given by

$$Area = \sum_{i=0}^{5} W_i \times L_i \tag{3.19}$$

The topology, defined in terms of constraints among the specifications is obtained from the above equations. All internal parameters of the topology, like W/L's, g_d's, g_m's of all transistors are removed to describe topology quantitatively. Based on the above assumptions and equations, simple CMOS OTA topology can be described as follow.

$$\left[\frac{GAIN \times (SR)}{(UGF)} \right] = \left[\frac{2\pi}{(\lambda_n + \lambda_p)} \right]$$

$$\left[\frac{PD}{(2 \times SR \times C_L)} \right] \geq [V_{dd} - V_{ss}]$$

$$\overline{dv^2_{nie}} \geq 2\left[\frac{8kT}{3} \left(\frac{1}{2\pi (UGF) C_L} + \frac{(SR)\Delta V}{8\pi^2 (UGF)^2 C_L} \right) + \frac{k_n k_{fn} (SR)}{4\pi^2 (UGF)^2 C_L f L_d^{\,2}} + \frac{k_p k_{fp} (SR)}{4\pi^2 (UGF)^2 C_L f L_d^{\,2}} \right]$$

$$AREA \geq 2\left[\left(\frac{\pi^2 (UGF)^2 C_L}{k_n (SR)} + \frac{(SR) C_L}{k_n \Delta V^2} + \frac{(SR) C_L k_p}{64\pi^2 C^2_{ox} L^4_d \tan(PM)} \right) \times L^2_d \right]$$

3.4.2 Miller Compensated Operational Transconuctance Amplifier

The schematics of basic two stage CMOS op-amp is shown in the Fig. 3.5. It consists of two stages, the first of which is a differential stage with PMOS input devices M1 and M2, and the NMOS current mirror M3 and M4, also acting as the active load. The second stage is a common source with M6 as the driver and M5 as the active load. The output of gain stage is connected to its input through the compensating capacitance C_c. Since C_c actually acts as miller capacitance of that stage, the op-amp is called a Miller compensated OTA. The mathematical equations that relate the performance specifications to the different device characteristics are given below.

1. Gain

The gain of basic two stage (BTS) op-amp is the product of the gain of the first stage and the second stage. The first stage is a simple OTA as described in subsection 3.3.2, the gain of which is given by

$$Gain_1 = -g_{m1}(r_{o2} \parallel r_{o4}), \tag{3.20}$$

$$Gain_2 = -g_{m6}(r_{o5} \parallel r_{o6}), \tag{3.21}$$

Thus, the overall gain can be expressed as

$$Gain = Gain_1 \times Gain_2 = g_{m1}g_{m6}(r_{o2} \parallel r_{o4})(r_{o5} \parallel r_{o6}) \tag{3.22}$$

Where g_{m1}, g_{m6} are the transconductances of M1, M6 and r_{o2}, r_{o4},r_{o5} and r_{o6} are the drain-source resistances of M2, M4,M5, M6 respectively.

2. Unity-gain frequency (UGF)

The unity-gain frequency of BTS is given by [36]

$$UGF = \frac{g_{m1}}{2\pi C_c}, \tag{3.23}$$

where C_c is the compensation capacitance.

3. ***Phase margin(PM)***
   The phase margin is given by the following expression.

$$PM = 90° - \tan^{-1}\left(\frac{UGF}{f_{nd}}\right), \tag{3.24}$$

where f_{nd} is the non-dominant pole created at the node 1 given by

$$= \frac{g_{m6}}{2\pi C_L},$$

where C_L is the output capacitance

4. ***Slew Rate(SR)***
   The slew rate is given by

$$SR = \frac{I_{bias}}{C_c}, \tag{3.25}$$

5. ***Power Dissipation***
   Power dissipation (PD) is given by

$$PD = (V_{DD} - V_{SS}) \times (I_{bias} + I_{d5} + I_{d7}) \tag{3.26}$$

6. ***Noise***

Each transistor contributes white noise and $1/f$ noise. The equivalent rms input noise voltage of a MOS transistor at any frequency is given by [36].

$$\overline{dv^2{}_n(f)} = \frac{8kT}{3}\frac{1}{g_m}df + \frac{K_F}{WL}\frac{df}{f}, \tag{3.27}$$

where $K_F = KF_F/C'^2_{ox}$, with KF_F being a technology parameter. In order to calculate the noise performance at low frequencies, all the capacitances are omitted. The different noise voltage sources present in an individual transistor can be clubbed

together to an equivalent input noise voltage source $\overline{(dv^2{}_{nie})}$ by using the following expression.

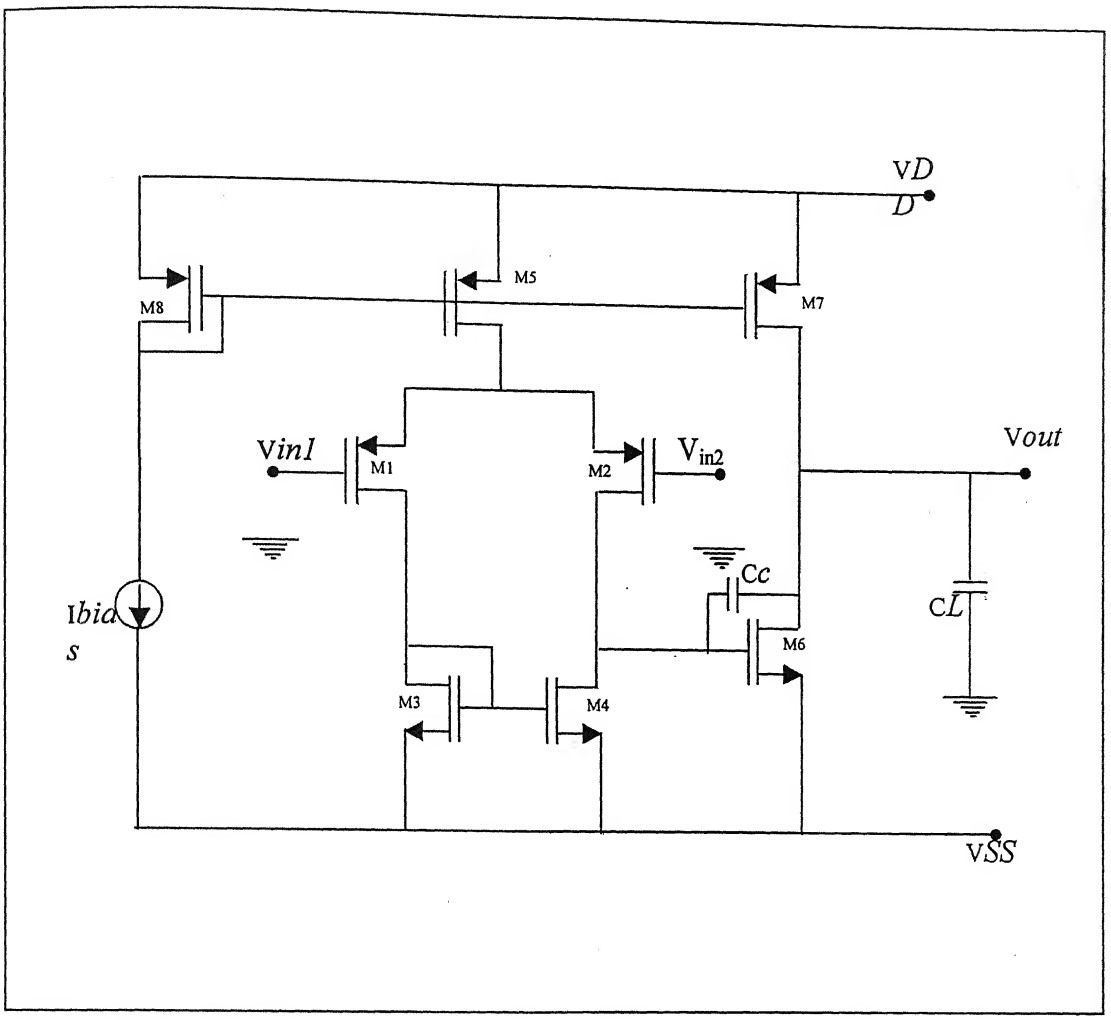


Fig.3.5: Schematic of a Miller compensated CMOS operational transconductance amplifier

$$\overline{dv^2{}_{nie}} = \sum_{i=1}^{n} \overline{dv^2{}_{ni}} \left(\frac{A_{vni}}{A_{vo}} \right)^2 , \qquad (3.28)$$

Where $\overline{dv_{nie}{}^2}$ is the equivalent noise of the i^{th} transistor referred to the input, A_{vni} is the gain of the i^{th} transistor from its input to the output, and A_{vo} is the overall gain of the circuit. It is observed that the noise due to M1, M2, M3 and M4 dominate the equivalent input noise. Thus it can be approximately given by the following expression.

$$\overline{dv^2_{nie}} \approx 2\left[\overline{dv^2_{n1}} + \overline{dv^2_{n3}}\left(\frac{g_{m3}}{g_{m1}}\right)^2\right] \tag{3.29}$$

7. *Area*

The total area is taken to be equal to the sum of the active areas taken by the individual transistors, and is given by

$$Area = \sum_{i=0}^{5} W_i \times L_i \tag{3.30}$$

. The topology, defined in terms of constraints among the specifications is obtained from the above equations. All internal parameters of the topology, like W/L's, g_d's, g_m's of all transistors are removed to define topology quantitatively. Based on the above assumptions and equations, Miller compensated CMOS OTA topology can be described as follow.

$$\left[\frac{GAIN \times (SR)^2}{(UGF)^2 \times (1+\tan(PM))}\right] = \left[\frac{10\pi^2}{(\lambda_n^{\,2} + \lambda_p^{\,2})}\right]$$

$$\left[\frac{PD}{(2 \times SR \times C_c + 2.5 \times SR \times C_L)}\right] \geq [V_{dd} - V_{ss}]$$

$$\overline{dv^2_{nie}} \geq 2\left[\frac{8kT}{3}\left(\frac{1}{2\pi(UGF)C_c} + \frac{3(1+\tan(PM))}{2(UGF)C_c}\right) + \frac{k_p k_{fp}(SR)}{2\pi^2(UGF)^2 C_c f L_d^{\,2}} + \frac{2.5 k_n k_{fn}(SR)}{4\pi^2(UGF)^2 C_c f L_d^{\,2}}\right]$$

$$AREA \geq \left[\left(\frac{4\pi\ (UGF)^2 C_c}{k_p(SR)} + \frac{2\pi^2(UGF)^2 C_L(1+\tan(PM))^2}{k_p(SR)} + \frac{(SR)C_c}{k_p \Delta V^2} + \frac{2.\pi^2(UGF)^2 C_L(1+\tan(PM))^2}{k_n(SR)} + \frac{2(SR)C_L}{k_p \Delta V^2}\right) \times L_d^{\,2}\right]$$

3.4.3 Folded Cascode Operational Tranconductance Amplifier

Folded cascode (FC) amplifier schematic is shown in the figure below. Transistor M5 and M6 are the cascode transistors. Transistor M7 and M9 form a cascoded current mirror. A separate biasing network (not shown in fig.) biases the cascode transistors, providing V_{b1} and V_{b2}. The current source I_{bias} and transistor M11 to M13 set the currents through all other transistors. The mathematical equations used for the computation of various performance specifications and topology definition are given below.

1. Gain

The only high impedence point in the circuit is the output node. All other node are at a resistance level of $1/g_m$. the output resistance R_{out} consists of a resistance towards M7, called $R_{out7}(=1/g_{out7})$ and one towards M6, called $R_{out6}(=1/g_{out6})$.

$$\begin{aligned} R_{out} &= \frac{1}{g_{out\,6} + g_{out\,7}}, \\ g_{out\,7} &= \frac{g_{o7} g_{o6}}{g_{m7}}, \\ g_{out\,6} &= \frac{g_{o6}(g_{o4} + g_{o1})}{g_{m6}}, \\ A_{vo} &= g_{m1} R_{out}. \end{aligned} \tag{3.31}$$

$$Gain_1 = \frac{g_{m1}}{\left[\left(\frac{g_{o7} g_{o6}}{g_{m7}}\right) + \left(\frac{g_{o6}(g_{o4} + g_{o1})}{g_{m6}}\right)\right]}. \tag{3.32}$$

Where g_m's are transconductances and gd's are the output conductances of the respective transistors.

2. Unity-gain frequency (UGF)

The unity-gain frequency of FC OTA is given by [36]

$$UGF = \frac{g_{m1}}{2\pi C_L}, \tag{3.33}$$

where C_L is the load capacitance.

3. ***Phase margin(PM)***

The phase margin is given by the following expression.

$$PM = 90^\circ - \tan^{-1}\left(\frac{UGF}{f_{nd}}\right), \tag{3.34}$$

where f_{nd} is the non-dominant pole created at the node 1 given by

$$= \frac{g_{m6}}{2\pi C_{L1}}, \tag{3.35}$$

where C_{L1} is the node capacitance due to transistor parasitic at source of transistor M6.

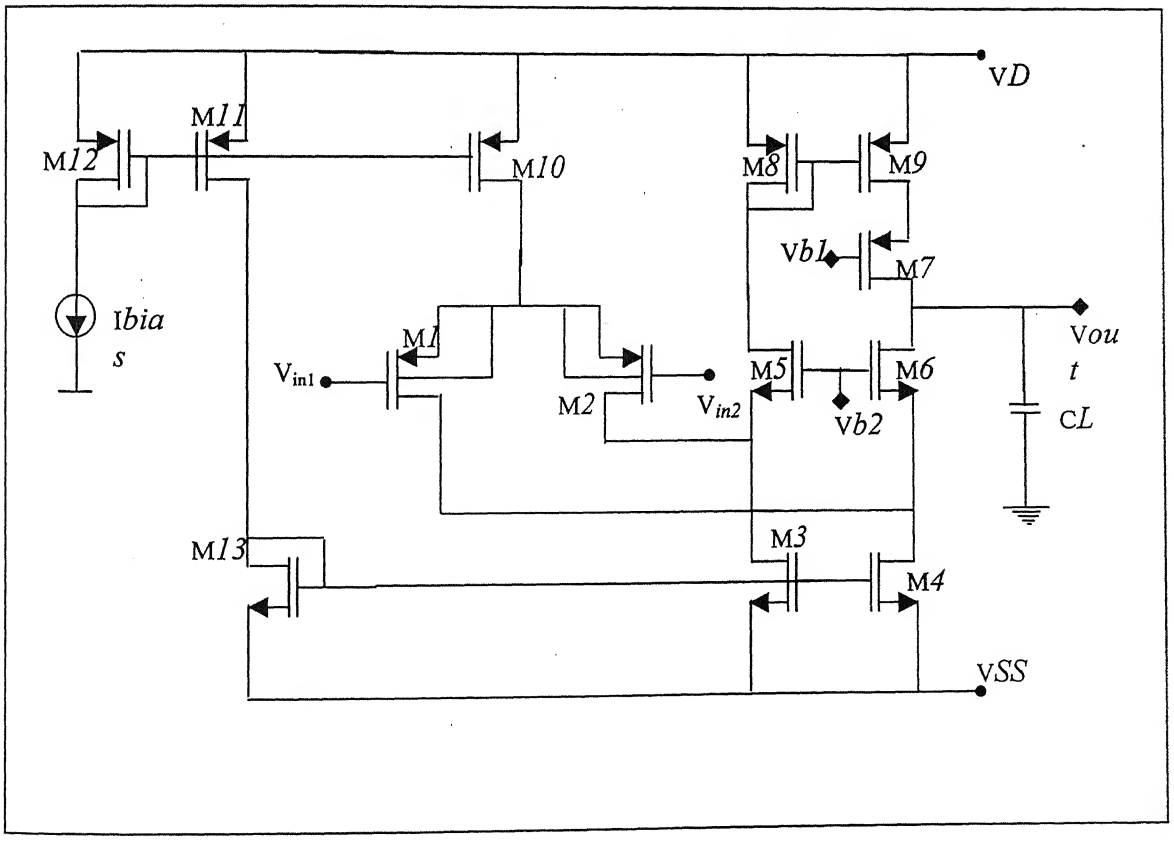


Fig.3.6: Schematic of a Folded Cacsode CMOS operational transconductance amplifier

4. ***Slew Rate(SR)***

The slew rate is given by

$$SR = \frac{I_{d10}}{C_L}, \tag{3.36}$$

5. ***Power Dissipation***

Power dissipation (PD) is given by

$$PD = (V_{DD} - V_{SS}) \times (2I_{bias} + I_{d5} + I_{d7}) \tag{3.37}$$

6. ***Noise***

The total output noise voltage power is the sum of the equivalent input noise voltage powers of each transistor, multiplied by their gain squared. Equivalent rms noise is given by as following expression.

$$\overline{dv^2_{nie}} = \sum_{i=1}^{n} \overline{dv^2_{ni}} \left(\frac{A_{vni}}{A_{vo}} \right)^2, \tag{3.38}$$

where is the equivalent noise of the i^{th} transistor referred to the input, A_{vni} is the gain of the i^{th} transistor from its input to the output, and A_{vo} is the overall gain of the circuit. It is observed that the noise due to M1, M3 and M8 dominate the equivalent input noise. Thus it can be approximately given by the following expression.

$$\overline{dv^2_{nie}} \approx 2 \left[\overline{dv^2_{n1}} + \overline{dv^2_{n3}} \left(\frac{g_{m3}}{g_{m1}} \right)^2 + \overline{dv^2_{n8}} \left(\frac{g_{m8}}{g_{m1}} \right)^2 \right] \tag{3.39}$$

7. ***Area***

The total area is taken to be equal to the sum of the active areas taken by the individual transistors, and is given by

$$Area = \sum_{i=0}^{13} W_i \times L_i \tag{3.40}$$

The topology, defined in terms of constraints among the specifications is obtained from the above equations. All internal parameters of the topology, like W/L's, g_d's, g_m's of all transistors are removed to define topology quantitatively.

Based on the above assumptions and equations, Folded Cascode CMOS OTA topology can be described as follow.

$$GAIN = \frac{4\pi(UGF)C_L(2k_n\Delta V + 2\pi k_1(UGF)\tan(PM))}{\left(2\pi(\lambda_n^{\,2} + \lambda_p^{\,2})(UGF)\tan(PM)C_{no}k_n\Delta V^2 + \lambda_n\lambda_{avg}(SR)C_L(2k_n\Delta V + 2\pi k_1(UGF)\tan(PM))\right)\Delta V}$$

$$PD \geq (V_{dd} - V_{ss})\left(2(SR)C_L + 2\frac{2\pi(UGF)\tan(PM)C_{no}k_n\Delta V^2}{(2k_n\Delta V - 2\pi k_1(UGF)\tan(PM))}\right)$$

$$\overline{dv^2}_{nie} \geq 2\left[\frac{8kT}{3}\left(\frac{1}{2\pi(UGF)C_L} + \frac{3(SR)}{4\pi^2(UGF)^2C_L\Delta V}\right) + \frac{2k_nk_{fn}(SR)}{4\pi^2(UGF)^2C_L fL_d^{\,2}} + \frac{2k_pk_{fp}(SR)}{4\pi^2(UGF)^2C_L fL_d^{\,2}}\left(\frac{3(SR)}{2\pi(UGF)}\right)^2 + \frac{2k_nk_{fn}}{4\pi^2(UGF)^2C_L f}\left(\frac{3(SR)}{2\pi(UGF)}\right)^2\right]$$

$$AREA \geq \left[\left(\frac{2\pi^2(UGF)^2C_L}{k_p(SR)} + \frac{36k_n(SR)C_L}{4\pi^2(UGF)^2\tan^2(PM)C_{ox}L_d^{\,4}} + \frac{5(SR)C_L}{2k_p\Delta V^2} + \frac{(SR)C_L}{4k_n\Delta V^2}\right) \times L_d^{\,2}\right]$$

3.5 RESULTS FOR OP-AMPS

Several experiments were performed with the program written to select one topology among three topologies described earlier. All the experiments are carried out for 3μm technology, process parameters, which are described in appendix-II.

Experiment 7

Table 3.9

Specification Name	Specification	Basic two Stage OTA	Simple OTA	Folded Cascode OTA
Gain(dB)	80.00000	104.737959	70.958339	130.535633
UGF(MHz)	5.000000	4.905198	3.066474	8.834193
Slew Rate(V/μs)	4.000000	6.531040	0.979543	9.636189
PM(deg)	60.00000	70.712349	62.725922	74.300041
Power Diss.(mW)	3.000000	2.938968	0.195909	1.927238
Active Area(μm2)	5000.000	2992.940118	1769.782432	3584.125219
Noise(ηV/√Hz)	150.0000	133.924516	98.194548	98.194548
%age Error	——	0.005392	21.257565	0.000000
Topology Selected	BASIC TWO STAGE OTA			

Experiment 8

Table 3.10

Specification Name	Specification	Basic two Stage OTA	Simple OTA	Folded Cascode OTA
Gain(dB)	60.0000	104.737959	70.958339	130.535633
UGF(MHz)	1.00000	4.905198	3.066474	8.834193
Slew Rate(V/μs)	1.00000	6.531040	0.979543	9.636189
PM(deg)	45.0000	70.712349	62.725922	74.300041
Power Diss.(mW)	5.00000	2.938968	0.195909	1.927238
Active Area(μm2)	5000.00	2992.940118	1769.782432	3584.211372
Noise(ηV/√Hz)	200.000	133.92452	98.19455	98.19455
%age Error	——	0.000000	0.006278	0.000000
Topology Selected	SIMPLE CMOS OTA			

Table 3.11

Specification Name	Specification	Basic two Stage OTA	Simple OTA	Folded Cascode OTA
Gain(dB)	120.000000	104.737959	70.958339	145.831090
UGF(MHz)	10.000000	4.905198	3.066474	6.998891
SlewRate(V/μs)	10.000000	6.531040	0.979543	9.804871
PM(deg)	45.000000	70.712349	62.725922	76.841438
Power Diss.(mW)	4.000000	2.938968	0.195909	1.960974
Active Area(μm2)	5000.000	2992.940118	1769.782432	4502.212260
Noise(ηV/√Hz	30.00000	133.92452	98.19455	98.19455
%age Error	——	22.815722	44.240124	1.356710
Topology Selected	FOLDED CASCODE OTA			

The Results for various experiments performed with the program written to select topology between fixed set of choices of op-amps are shown in the table above. The following observations can be made on the basis of above results.

- For small gain (<60dB) and small UGF (<1MHz), simple CMOS OTA is best choice among the three topologies. Although the other two topologies also satisfy these requirements, they require more active area and higher power dissipation in general.
- For large gain (>120dB) and high UGF (>10MHz), folded cascode CMOS OTA is a better choice as it is only topology which satisfies the required specifications.
- For moderate gain (≈80dB) and medium UGF (≈5MHz), miller compensated CMOS OTA requires relatively less area as compared to folded cascode CMOS OTA.

These observations again are in agreement with what is commonly known about op-amp topologies. The present topology selection procedure being based on well-define analytical equations has the advantage being much more precise as compare to hueristics based selection procedure. It has a further advantage of being

invarient with respact to changing technology. Unlike other methods where a numerical value deduced from many design cycles is needed, in the present approach only readily available process parameters need to be changed.

CHAPTER 4

CONCLUSION AND FUTURE SUGGESTIONS

It is a well known fact that optimization at the highest level of abstraction in the design process yields the maximum gain in terms of performance parameters. In cell level analog synthesis, this means that topology selection is the first design step which must be optimized to get best performance.

This work was started with an aim to build a synthesis tool to select topology among the fixed set of topologies. A new approach has been presented for selection of topology from a fixed set of alternatives. The basis of the new approach is in the new definition of a topology, which is characterized as a set of analytical equations that describe the constraints among the specifications. Topology selection is done by determining the topology, which while satisfying all the constraints has minimum area or some other metric like power dissipation or minimum noise. It is shown that this approach encompasses within it the traditional qualitative rule-based topology definition and selection methods. The validity of the approach was demonstrated through the examples of well-known CMOS current sources and op-amps like, Miller compensated CMOS OTA, simple CMOS OTA and Folded cascode CMOS OTA. The results obtained were in agreement with what is commonly known about these

topologies. For current sources, the results were also verified through complete design of the current sources. In order to add more number of circuit topologies, little modifications in the module is necessary, however extensive circuit knowledge is required.

FUTURE SUGGESTIONS

The following modifications and additions are required to make a complete synthesis tool, which would easy to handle by a novice designer.

- The module that does the design has to be added. Further a module for specification modifications has to be added.
- Extend the work to more complicated circuits like A/D converter, Phase Locked Loop (PLL), the switched capacitor filter, etc. A suitable methodology has to be developed to deduce the specifications of basic building blocks from the specifications of the more complex analog blocks.
- Develop tools and interfaces that would make it possible even for the user to add a new topology to the topology library.
- Build an interface with the symbolic simulator e.g., ISAAC or SAPWIN, which will provides the analytical equations required for topology selection.

REFERENCES

1. C. Toumazou, and C. A. Makris, "Analog IC design automation: Part I-Automated circuit generation: New concepts and methods," *IEEE Trans. Computer Aided Design*, vol. 14, no. 2, pp. 218-238, Feb. 1995.
2. Torralba, J. Chavez, and L.G. Franquelo, " FASY: A fuzzy logic based tool for analog synthesis", *IEEE Trans. Computer-Aided Design*, vol. 15, no. 7, pp. 785-793, July. 1996.
3. Prabir C. Maulik, L. Richard Carley and Rob A. Rutenbar, " Integer Programming Based Topology Selection of Cell-Level Analog Circuits" , *IEEE Trans. Computer Aided Design*, vol. 14, no. 4, pp. 401-412, April 1995.
4. Y. P. Tsividis, "Analog MOS integrated circuits-Certain new ideas, trends and obstacles," *IEEE J. Solid State Circuits,* vol. SC-22, no.3, pp.317-321, June 1987.
5. J. P. Harvey, M. I. Elmasry, and B. Leung, " STAIC: An interactive framework for synthesizing CMOS and BiCMOS analog circuits", *IEEE Trans. Computer Aided Design*, vol. 11, no. 11, pp. 1402-1417, Nov. 1992.
6. D. C. Stone, J. E. Schroder, R. H. Kaplan, and A. R. Smith, "Analog CMOS building blocks for custom and semicustom applications," *IEEE J. Solid State Circuits,* vol. SC-19, no. 1, pp.56-61, Feb. 1984.
7. T. Pletersek, J. Trontelj, L. Trontelj, I. Jones, and G. Shenton, " High performance designs with CMOS analog standard cells," *IEEE J. Solid State Circuits,* vol. SC-21, no. 2, pp.215-222, Apr. 1986.
8. M. J. S. Smith *et al.*, "Cell libraries and assembly tools for analog/digital CMOS/BiCMOS application specific integrated circuit design," *IEEE J. Solid State Circuits,* vol. SC-24, no. 5, pp. 1419-14325, Dec. 1989.
9. R. Harjani, R. A. Rutenbar, and L. R. Carley, "OASYS: A framework for analog circuit synthesis", *IEEE Trans. Computer-Aided Design*, vol. 8, no. 6, pp. 680-691, June. 1990.
10. F. El-Turkey and E. E. Perry, "BLADES: An artificial intelligence approach to analog circuit design", *IEEE Trans. Computer-Aided Design*, vol. 8, no. 12, pp. 1247-1265, Dec. 1989.

22. J. M. Shyu and A. Sangiovanni-Vincetelli, "ECSTASY: A new environment for IC design optimization", in *Proc. IEEE Inter. Conf. Computer-Aided Design (ICCAD),* 1988, pp.484-487.

23. J.C. Lai, J.S. Kueng, H. J. Chen, and F. J. Fermandez, "ADOPT- A CAD tool for analog circuit design, *IEEE Circ. Devices*, pp.29-30, Mar. 1988.

24. S. Ochotta, R.A. Rutenbar, and L.R. Carley, " Synthesis of high performance analog circuits in ASTRX/OBLX", *IEEE Trans. Computer Aided Design*, vol. 15, no. 3, pp. 273-293, Mar. 1996.

25. M. Fares and Bozena Kaminska, " FPAD: A Fuzzy Nonlinear Programming Approach to Analog Circuit Design", *IEEE Trans. Computer Aided Design*, vol. 14, no. 7, pp. 785-793, Jul. 1995.

26. P. Mandal and V. Viswanathan, " A new approach for CMOS Op-Amp Synthesis", *12th International Conference on VLSI Design*, pp.189-194, Jan. 1999.

27. P. C. Maulik, L. R. Carley and D. J. Allstot, "Sizing of cell level analog circuits using constrained optimization techniques", *IEEE J. Solid-State Circuits*, vol. SC-28, No. 3, pp. 233-241, March, 1993.

28. P. R. Gray and R .G. Meyer, "MOS operational amplifer design - A tutorial overview", *IEEE J. Solid-State Circuits*, vol. Sc-17, no. 6, pp. 969-982, Dec. 1982.

29. K. D. Peterson, and R. L. Gieger, " Area/Bandwidth Tradoffs for CMOS Current Mirrors" *IEEE Trans. Circuits & Systems*, vol. CAS-33, no. 7, pp. 667-669, Jul. 1986.

30. G. G. E. Gielen, H. C. C. Walscharts, and W. M. C. Sansen, "ISAAC: A symbolic simulator for analog integrated circuits", *IEEE J. of Solid-State Circuits*, vol. 24, no. 6, pp. 1587-1596, Dec. 1989.

31. L. R. Carley and R. A. Rutenbar, "How to automate analog IC design", *IEEE Spectrum,* vol. 25, pp.26-30, Aug. 1988.

32. G. Kelson, "Design automation techniques for analog VLSI," *VLSI Design*, Jan. 1985, pp. 78-82.

33. J. H. Huijsing, R. J. Plassche and W. Sansen, *Analog Circuit Design*, Kluwer Academic Publishers, London, 1993.

34. P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, John Wiley and Sons, New York, 3rd Edition, 1993.

35. R. Gregorian and G. C Temes, *Analog MOS Integrated Circuits for Signal Processing*, New York: Wiley, 1984.

36. K. R. Laker and W. M. C. Sansen, *Design of Analog Integrated Circuits and Systems*, McGraw-Hill, Hightstown, 1994.

37. R. L. Geiger, P. E. Allen, and N. R. Strader, *VLSI Design Techniques for Analog and Digital Circuits*, New York: McGraw-Hill, 1990.

38. M. Ismail and J. Franca, *Introduction to Analog VLSI Design Automation*, Kluwer Academic Publishers, London, 1990.

39. A. A. Antao, and A. J. Brodersen, "ARCHGEN: Automated synthesis of analog systems", *IEEE Trans. VLSI Systems*, vol. 3, no. 2, pp. 231-244, Jun. 1995.

40. A. A. Antao and A. J. Brodersen, " Techniques for synthesis of analog integrated circuits", *IEEE Design & Test of Computers*, vol. 14, no. 2, pp. 8-17, Mar. 1992.

41. H. C. Yang, M. A. Deyeh, and David J. Allstot, " Small Signal Analysis and Minimum settling time Design of a one stage Folded-Cascode CMOS Operational amplifier", *IEEE Trans. Circuits & Systems*, vol. 38, no. 7, pp. 804-807, Jul. 1991.

42. Bedrich J. Hosticka ," Improvement of the Gain of MOS Amplifiers" , *IEEE J. Solid-State Circuits*, vol. Sc-14, no. 6, pp. 1111-1114, Dec. 1979.

43. Eric A. Vittoz. ," The Design of High Performance Analog Circuits on Digital CMOS Chips", *IEEE J. Solid-State Circuits*, vol. Sc-20, no. 3, pp. 657-665, Jun. 1985.

44. A. R. Feldman and P. R. Gray ,"High-Speed ,Low -Power Sigma-Delta Modulators for RF Baseband Channel Applications", *Phd Dissertation, Deptt. of Electrical Engg. and Compuer Science*, Univ. of California Berkeley.

45. P. Mandal and V. Visvanathan ,"A Self Biased High Performance Folded Cascode CMOS Op-Amp " ,*10th International Conference on VLSI Design*, pp 429-434, January 1997.

46. V. R. Babu, and B. Mazhari," An Expert System Approach to Analog Circuit Synthesis", *M.Tech Dissertation, Dept.of Electrical Engg.*, IIT Kanpur, March 1996.

47. K. Swings, S. Donnay, and W. Sansen, "HECTOR: A hierarchical topology program for analog circuits based on a declarative approach to circuit modeling ", *Proc. CICC*, pp. 5.3/1-4, 1991.

48. K. Deb,"Optimization for engineering design algorithms and examples", *Prentice-Hall of India* . 1998.

49. K. Deb, R.B.Agrawal,"Simulated Binary Crossover countinuous search space",*complex systems,* vol. 9, pp.115-148, 1995.

50. Microsim Corporation, "Users Guide-Microsim® PSPICE® Optimizer Analog Performance Optimization Software", version 7.1. 1996.

APPENDIX-I

Genetic Algorithm Concepts

Genetic algorithm (GA) is computerized search and optimization algorithm based on the mechanics of natural genetics and natural selection. GA mimics the survival of fittest principle of nature to make a search process. Therefore GA's are naturally suitable for maximization type problem. Present problem is of minimization type, but it is converted into maximization type. In general, fitness function F(x) is first derived from the objective function and used in successive genetic operations. The operation of GA does begin with a population of random strings representing design or decision variables. Therefore each string is evaluated to find the fitness value. The population is then operated by three main operators'– reproduction, crossover and mutation–to create new population of points. The new population is again evaluated and tested for termination. If the termination criteria are not met, the population is iteratively operated by the above three operators and evaluated. The procedure is continued until the termination criterion is not met. One cycle of these operations and the subsequent operations and the evaluation procedure is known as a generation in GA's terminology. More information about genetic algorithm and literature, one can check with the [48].

GA Operators

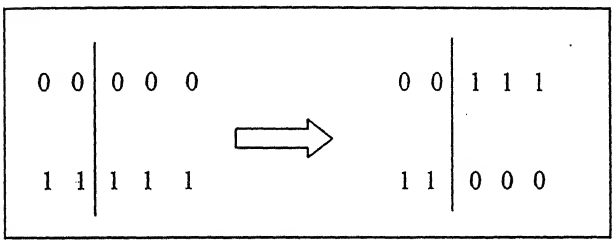
Reproduction is usually the first operator applied on a population. Reproduction selects good strings in a population and forms a mating pool. The commonly used reproduction operator is the proportionate reproduction operator where a string is selected for the mating pool with a probability proportional to its

F_i. Therefore, probability for selecting the i^{th} string is given by [49]

$$p_i = \frac{f_i}{\sum_{j=1}^{n} f_j},$$

where n is population size.

In reproduction, good strings in a population are probabilistically assigned a larger number of copies and a mating pool is formed. In crossover operator, exchanging information among strings of the mating pool creates new strings. In most crossover operators, two strings are picked from the mating pool at random and some portions of the strings are exchanged between the strings. A single-point crossover operator is performed by randomly choosing a site along the string and by exchanging all bits on the right side as shown below.



The two strings participating in the crossover operation are known as parent strings and resulting strings are known as children strings. A crossover operator is mainly responsible for the search of new strings, even though a mutation operator is also used for this sparingly. The mutation operator changes from 1 to 0 and vive versa with a small mutation probability, p_m. the bit-wise mutation is performed bit by bit by flapping a coin with probability p_m. if at any bit outcome is true then bit is altered; otherwise a bit is kept unchanged. The need for mutation is to create a point in the neighborhood of the current point, thereby achieving a local search around the current situation. The mutation is also used to maintain diversity in the population. For example, consider the following population having four eight strings.

01101101

00111101

Notice that all four strings have 0 in the left most bit position. If the true optimu solution requires 1 in that position, then neither reproduction nor crossover operat described above will be able to create 1 in that position, the inclusion of mutatic introduces some probability(Np_m) of turning 0 to 1.

These three operators are simple and straightforward. The reproductic operator selects good strings and crossover operator recombines the good substrin together to hopefully create better substring. The mutation operator alters a strir locally to hopefully create better string. Even though none of these claims a guaranteed and /or tested while creating a string, it is expected that if bad strings a created they will eliminated by reproduction operator in the next generation and good strings are created, they will increasingly emphasized.

A Simple Genetic Algorithm

Given a clearly defined problem to be solved and a bit string representation for candidate solutions, a simple genetic algorithm works as follow [49].

1) Choose a coding to represent problem parameters, a selection operator, a crossover operator, a mutation operator. Choose population size, n , crossover probability, p_c, and mutation probability, p_m. Choose a maximum allowable generation number t_{max}. Set $t = 0$.
2) Evaluate each string in the population. Calculate the fitness of each string in the population.
3) If $t \geq t_{max}$ or other termination criteria is satisfied, **Terminate.**
4) Perform the following steps on the current population.
   a) Select a pair of parent chromosomes from the current problem, the possibility of selection being an increasing function of fitness. Selection is done "with replacement" meaning that the same chromosomes can be selected more than once to become a parent.
   b) With probability p_c (the "crossover probability" or "crossover rate"), crossover the pair at a randomly chosen point(chosen with uniform probability) to form two offspring. If no crossover takes place, from two

offspring which are exact copies of their respective parents. (Here the crossover rate is defined to be probability that two parents will cross over a single point. There are also multi-point crossover versions of the GA in which the crossover rate for a pair of parents is the number of points at which crossover takes place.)

c) Mute the two offspring at each locus with probability p_m (mutation probability or mutation rate) , and place the resulting chromosomes in the new population. If n is odd, one new population member can be discarded at random.

5) Replace the current population with the new population.

6) Go to step 3.

APPENDIX-II

The MOS Technology File

A set of process parameters for typical silicon –gate n-well CMOS process with 3μm technology, which is used in the selection of all MOS circuit topologies in the present work.

Sl. No.	**Parameter**	Symbol	*Value*	
			n-channel transistor	*p-channel transistor*
1.	Substrate doping(atoms/cm^3)	N_A, N_D	1×10^{15}	1×10^{16}
2.	Gate oxide thickness(A°)	t_{ox}	400	400
3.	Metal-silicon work function(V)	ϕ_{ms}	-0.7	-0.1
4.	Channel mobility(cm^2/V-sec)	μ_n, μ_p	700	350
5.	Minimum drawn channel length(μm)	L_{drawn}	3	3
6.	Source, drain junction depth(μm)	X_j	0.6	0.6
7.	Source, drain side diffusion(μm)	L_d	0.3	0.3
8.	Overlap capacitance per unit gate width (fF/μm)	C_{ol}	0.35	0.35
9.	Threshold adjust effective depth(μm)	X_i	0.3	0.3
10.	Threshold adjust effective surface concentration(atosm/cm^3)	N_{si}	2×10^{16}	0.9×10^{16}
11.	Nominal threshold voltage(V)	V_t	0.7	-0.7
12.	Poly-silicon gate doping	N_{dpoly}	10^{20}	10^{20}

	concentration(atoms/cm^3)			
13.	Poly gate sheet resistance(Ω/□)	R_S	20	20
14.	Source/drain-bulk junction capacitance per unit source/drain area (fF/μm^2)	C_{j0}	0.08	0.20
15.	Source/drain-bulk junction capacitance grading coefficient	n	0.5	0.5
16.	Source/drain-periphery capacitance per unit source drain periphery (fF/μ)	C_{jsw0}	0.5	1.5
17.	Source/drain-periphery capacitance grading coefficient	n	0.5	0.5
18.	Souce, drain junction built-in potential (V)	ψ_o	0.65	0.65
19.	Surface state density(atoms/cm^3)	N_{ss}	10^{11}	10^{11}
20.	Channel length modulation parameter (μ/V)	dX_d/dV_{DS}	0.2	0.1
21.	Flicker noise coefficient($V^2\mu m^{2+}$)	KF	10^{-8}	5^{-10}